SERVICE MANUAL

KENWOOD

DP-1100B
DP-1100II

COMPACT DISC PLAYER

NOTE: Please replace this service manual with the old DP-1100's manual (B51-1592-00). This manual has all descriptions for DP-1100 and DP-1100II.

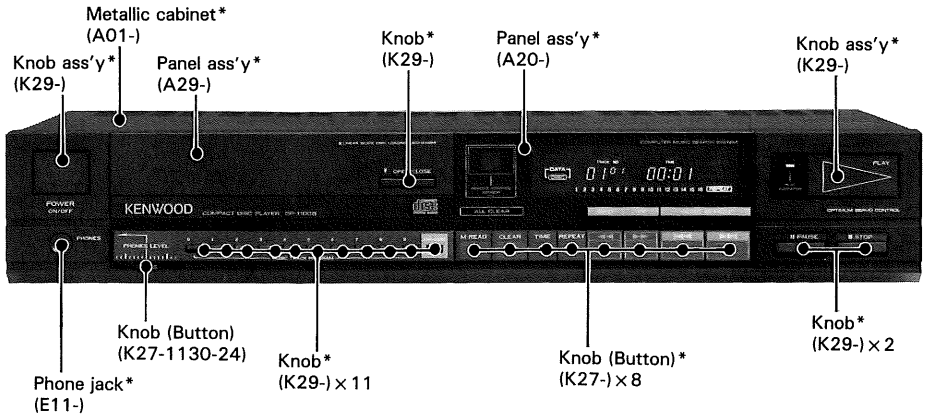


Photo is DP-1100B
*Refer to Parts List on page 177.

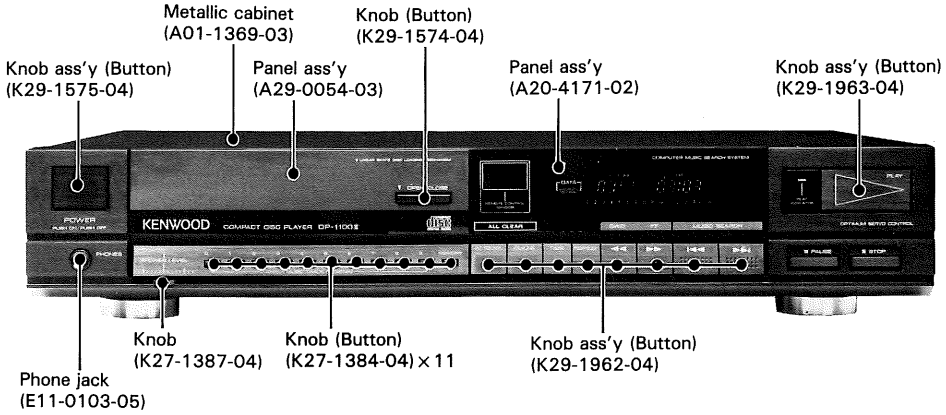


Photo is DP-1100II
*Refer to Parts List on page 191.

TRIO-KENWOOD Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040.10, Chapter I, Subchapter J.

DANGER: Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

MEANING OF ABBREVIATIONS

AFC: Disc motor speed control signal output from IC8 on process PCB

APC: Disc motor phase control signal output from IC8 on process PCB

BCK: Clock pulse on which music data is sent to D/A converter (Bit clock pulse)

CK4M: Clock signal of about 4 MHz for microprocessor (the signal resultant from 1/2 frequency division of X'tal OSC 8.4672 MHz)

CK88: About 88 kHz signal which is identical with signal WDCK (word clock pulse) output from IC6 on process PCB. It is used as clock signal for IC15 on servo PCB or as pseudo EFM signal.

CLS: Switch to inform opened or closed tray state. It is shorted with tray closed. (''L'' with tray closed)

CLV: Circuit which makes the linear velocity of disc motor constant to provide constant reading rate of disc data.

DATA 12 and DATA 21: Signals for data communication (transmission and reception) between CPU 1 and CPU 2.

DATA: Signal line on which data is sent from process PCB to D/A converter.

DCON: Signal which is output from IC15 on servo PCB. It is normally ''H'' and becomes ''L'' when RF signal is lowered in level due to disc flaw. (Dropout control)

DIN: Signal line on which positional data of disc flaw is transmitted between disc flaw position memory circuit and IC15 on servo PCB.

DISK: Disc motor drive signal

DOCK: Clock pulse output from IC15 on servo PCB to disc flaw position memory circuit. It is a six times amplified signal of FGS. (Dropout clock pulse)

DOK: With disc provided, this pulse output is ''L''. Q1 on servo PCB detects the presence or absence of disc. (Disc OK)

DSG: Refer to ''IC15 pin function'' on page 68.

EFM, EFM 1 and EFM 0: Eight-to-Fourteen-Modulation signals. These are high-frequency signals or RF signals given from optical pickup.

EMPH: Pre-emphasis signal output from IC8 on process PCB.

F.COIL and T.COIL: Focusing and tracking coils control signals.

FE or F.E: Focus error signal

FG4: Signal resultant from 1/30 frequency division of signal DOCK. It controls disc motor drive signal.

FGS: IC15 input pin of FG signal from disc motor.

FOK: Focus servo control signal. Servo ON with signal FOK ''L''.

FOKG: Refer to ''IC15 pin function'' on page 69.

FSRH or FSRCH: 2 Hz signal to detect just focusing point. It moves the pickup actuator up and down.

IRQ: Interrupt control I/0 pin between CPU 1 and CPU 2 (Interrupt request)

KGC: Inversion signal of signal RFG in IC15. It is normally ''L'' and ''H'' during kick of motor.

KICFB or KCIF: Refer to ''IC15 pin function'' on page 70.

LDC: Refer to ''IC15 pin function'' on page 69.

LRCK: Signal output from IC6 on process PCB. It indicates whether output data is for L-ch or R-ch.

MODE 4: IC15 control signal which is output from main CPU. (Refer to page 70.)

M5P: Disc motor ON/OFF control signal.

MUTE: Music signal muting signal.

OPEN: Switch which turns ON (''L'') with tray open to inform opened tray state.

OPNS: Refer to ''IC15 pin function'' on page 68.

PLAY: Refer to ''IC15 pin function'' on page 69.

PLCK: Refer to ''IC15 pin function'' on page 71.

PU or P.U: Pickup.

PUD: Refer to ''IC15 pin function'' on page 68.

PUFB: Inversion signal of signal PUFF in IC15.

RES: CPU initialize signal

RFES: Refer to ''IC15 pin function'' on page 69.

RFG: Refer to ''IC15 pin function'' on page 70.

RFOK: This output becomes ''L'' when RF signal from pickup is input to IC10 (V2).

RMC: Output signal from remote control signal amplifier

S1 and S2: Pickup output signals emitted from preamplifier on mechanism PCB.

SCK: Clock pulse for communication between CPU1 and CPU 2. (Serial clock pulse)

SLT: Switch which turns ON (''L'') with pickup at innermost track.

START or STAT: IC12 control signal to enable SVC operation by main CPU. (IC12 ON at ''H'')

SVC (A, B, C and INH): Servo control

TE or T.E: Tracking error signal or tracking monitor pin

TEG 1 and TEG 2: Refer to ''IC15 pin function'' on page 68.

TEOP and TEON: Refer to ''IC15 pin function'' on page 68.

TEP: Refer to ''IC15 pin function'' on page 68.

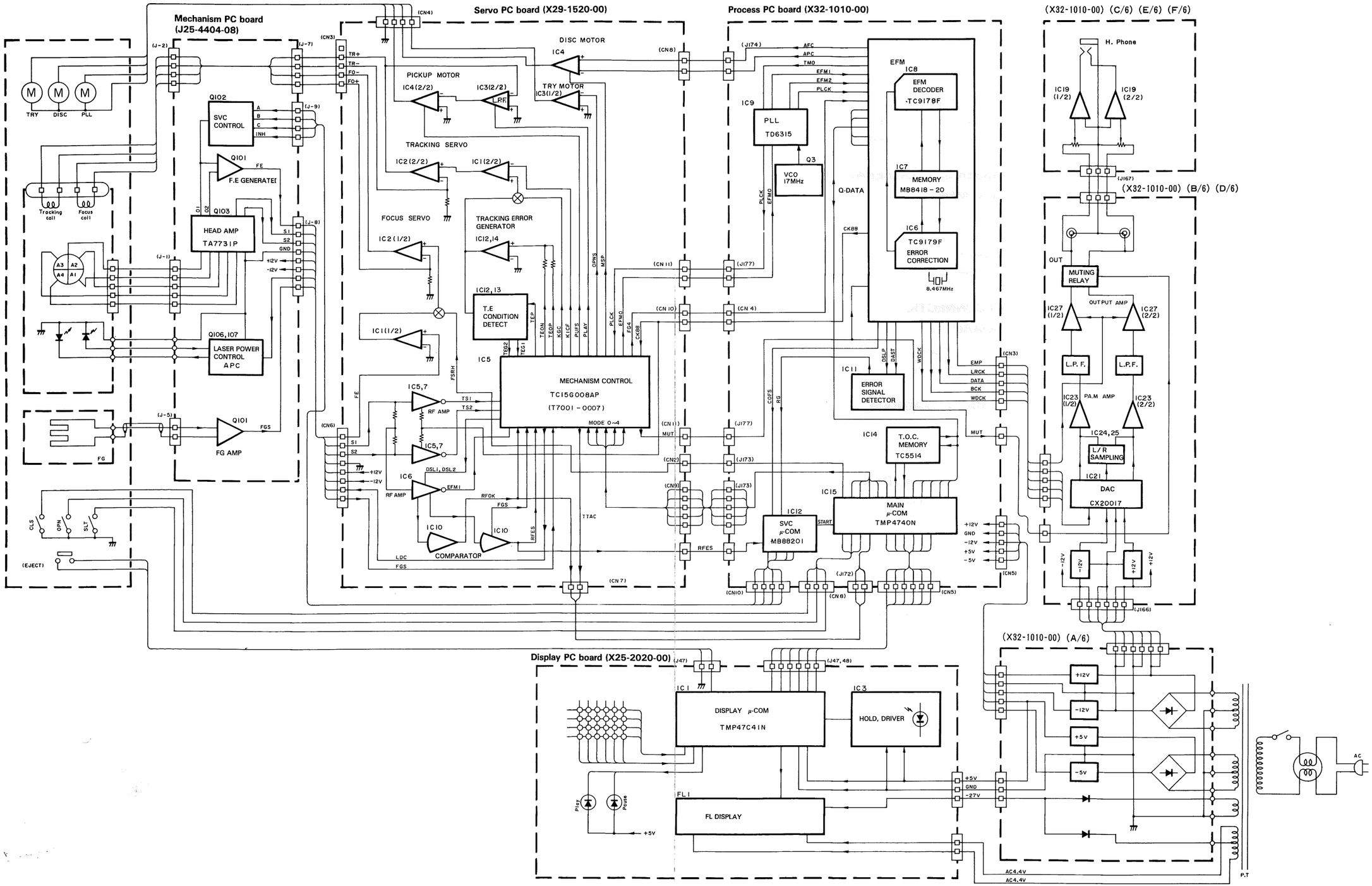
TES: Refer to ''IC15 pin function'' on page 68.

TRAY or TRY: Disc tray or tray drive signal

TTAC: Refer to ''IC15 pin function'' on page 68.

WDCK: Signal output from IC6 on process PCB. Its frequency is twice that of signal LRCK.

I. BLOCK DIAGRAM



II. FUNDAMENTALS

1 FUNDAMENTALS

1-1 SAMPLING

An analog voltage is continuous in respect to time, and has a value at each time of t_1, t_2, t_3, etc. as shown in Fig. 1.1 and as well a value at any time between t_1 and t_2.

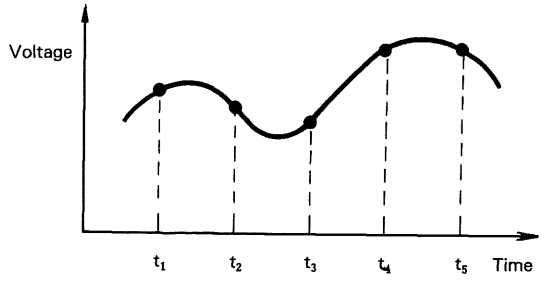


Fig. 1.1

If an analog voltage is represented corresponding to a code system, the analog voltage over the definite time range of t_1 to t_2 is made of the indefinite number of codes. In order to transmit a digital signal corresponding to the voltage at t_1, it needs a definite time length, but when transmitting indefinite codes, the transmission does not end forever.

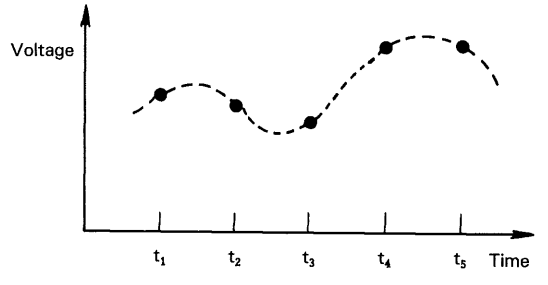


Fig. 1.2

Therefore, in case where an analog voltage is converted to a coded system, analog voltages at timings with some interval are only converted as shown in Fig. 1.2. With such a process, the definite number of codes corresponding to the definite timings, for example, five codes for the time interval t_1 to t_5 are produced.

When having transmitted codes described in Fig. 1.2, only five codes can be received at the receive side between t_1 and t_5. The number of voltage values reproduced thereby is only five, any voltage at timings except t_1, t_2, t_3, etc. cannot be determined.

However, if the frequency component (20 kHz) of the original analog signal is less than the value (44.1 kHz) depending upon the time interval between timings t_1, t_2, t_3, etc. at which coding is staged, even the value for non-transmitted portions can be reproduced. To pick up analog values at a fixed time interval by such a process is called "sampling".

1-2 QUANTIZATION

Fig. 1.3 indicates one example where analog signals ranging from 0V to 10V are converted to 11-step voltage values of 0V, 1V, 2V,...,9V and 10V via round-off. With this conversion, preparation of only 11 kinds of codes is needed. To convert an analog signal to a kind of a digital signal with the process of round-off or the like is called "Quantization".

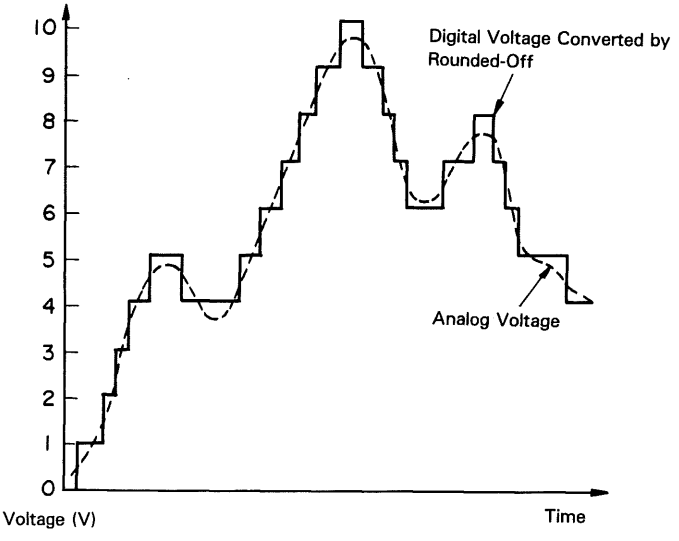


Fig. 1.3

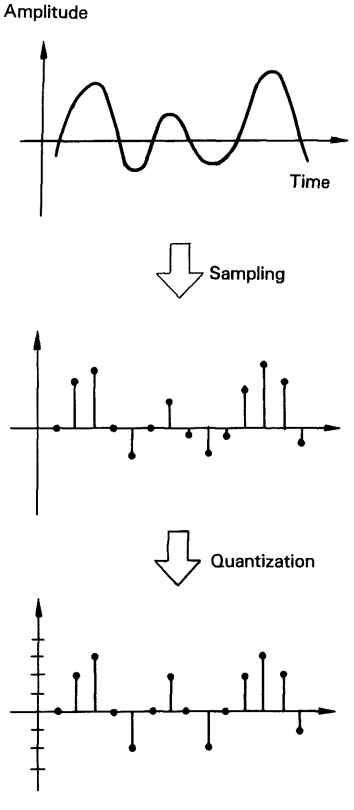


Fig. 1.4

II. FUNDAMENTALS

1-3 SAMPLING THEOREM

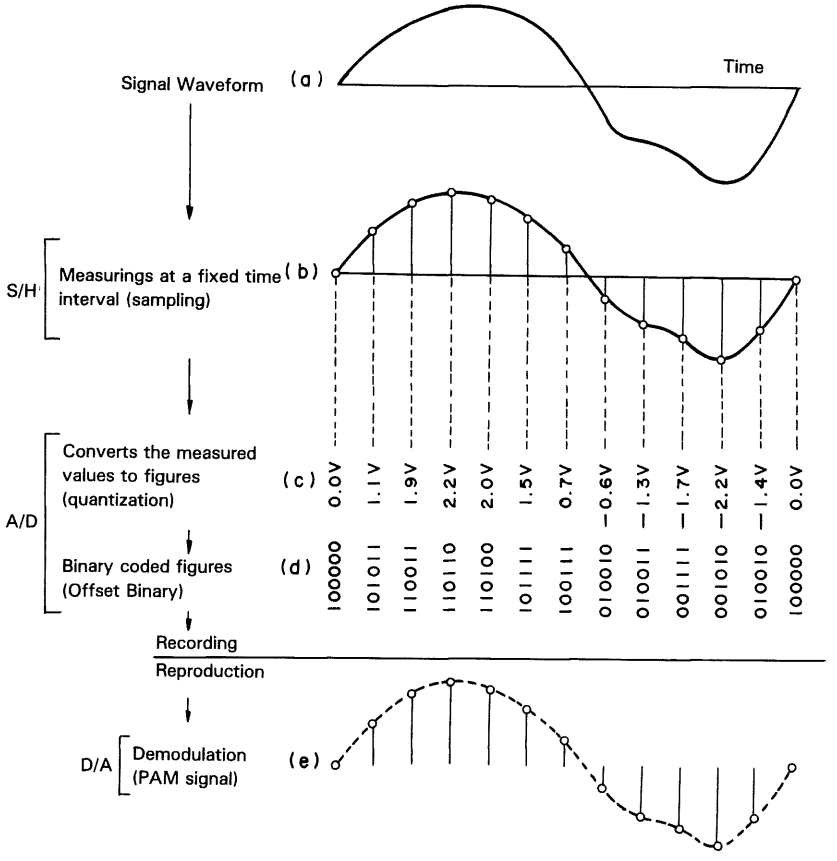


Fig. 1.5

The frequency of picking up an analog signal, for example, 50,000 times per second, is called "a sampling frequency. It is proven that if sampling is conducted at the rate larger than a certain value, the original waveform can be reproduced just the same to an inch. This is called "a sampling theorem".

Sampling Theorem: If sampling is conducted at the frequency (44.1 kHz) which is over double the maximum frequency (20 kHz) in a spectrum of a signal, the original waveform can be completely reproduced.

II. FUNDAMENTALS

1-4 QUANTIZING NOISES

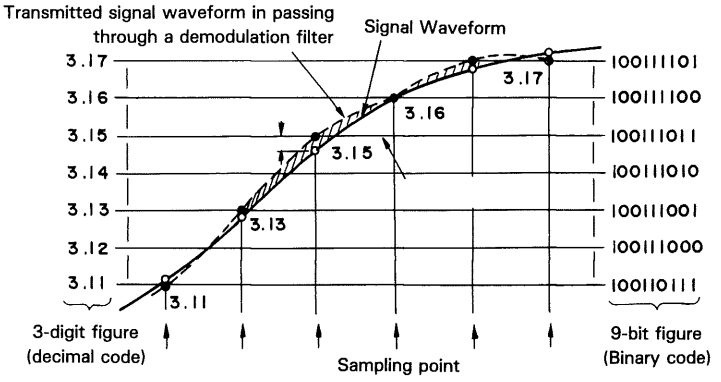


Fig. 1.6

A rounding error is caused by quantization at sampling points as described in 1-2, and seeing Fig. 1.6 it can be thought that this rounding error is created as a distortion or noise. This noise is of the nature different from noises emitted from an analog system, being called "a quantization noise".

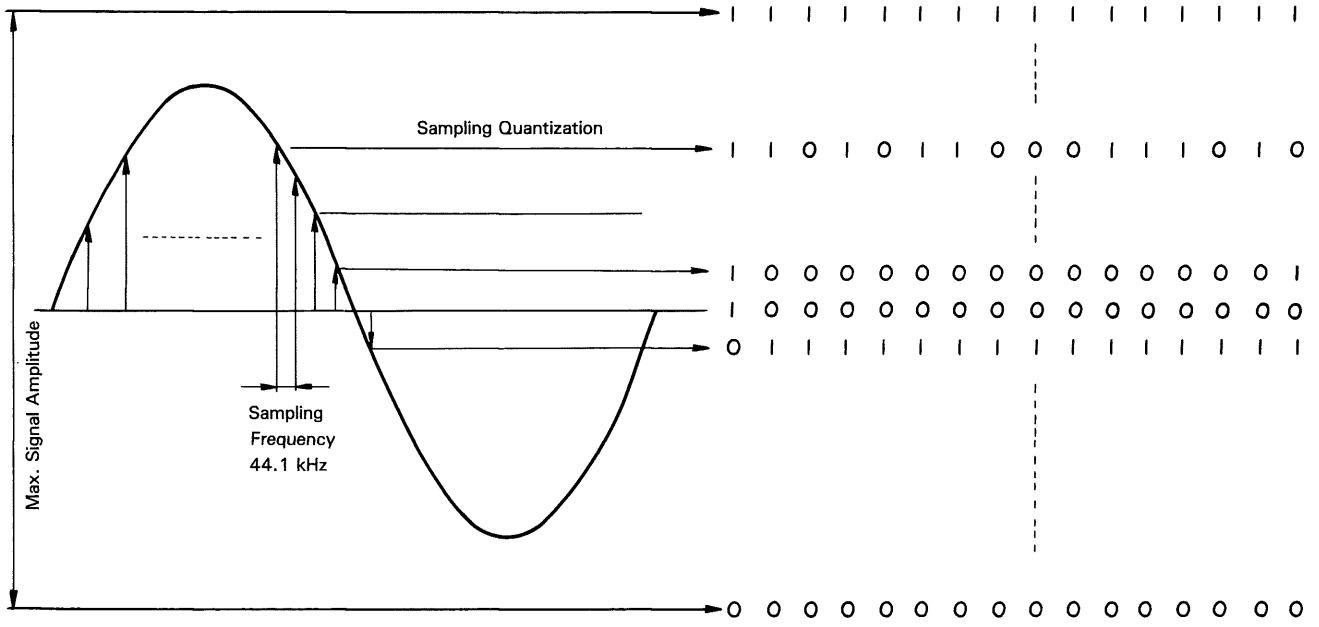


Fig. 1.7

The ratio of a quantizing noise against the maximum value of the signal in a binary-coded 16-bit system is plotted in respect to a sinusoidal wave input as shown in Fig. 1.7.

If a 16-bit code is used in quantizing one sampled value, the number of steps which can be taken, i.e., the quantizing number N is given as follows:

$N = 2^{16} = 65536$

When making the amplitude of 0 to V corresponding to this, the width E_0 of one quantization step is given by:

$E_0 = V/(N-1)$

Therefore, the amplitude of a quantizing noise is E_0 at the peak-to-peak value, so that the noise power N_Q is:

$$NQ = \frac{2}{E_0}\int_0^{\frac{E_0}{2}} X^2 dX = \frac{E_0^2}{12}$$

II. FUNDAMENTALS

On the other hand, supposing that an input signal is a sinusoidal wave whose amplitude at the peak-to-peak value is V, the signal power S is:

$$S = \frac{1}{2\pi}\int_0^{2\pi} \left(\frac{V}{2}\sin X\right)^2 dX = \frac{V^2}{8}$$

Therefore, the power ratio is:

$$\frac{S}{N_Q} = \frac{V^2}{8} \Big/ \frac{E_o^2}{12} = \frac{3}{2}(N-1)^2$$

$$D = 10\log\frac{S}{N_Q} = 10\log\frac{3}{2}(2^{16}-1)^2 \fallingdotseq 98\,dB$$

1-5 EFM (EIGHT TO FOURTEEN MODULATION)

To convert a level of an analog signal at every interval of a fixed period (1/44.1 kHz = 22.7 μs), as described in 1-4, to a binary code (1 and 0) after quantization is called a "PCM" (Pulse Code Modulation).

PCM has various kinds of modulation systems, but here a Sony and Philips jointly developed new system, called EFM, used for DAD is described.

Role of Margin Bits

The purpose of the margin bits is to reduce a DC component and low frequency components by adding three additional bits to the signals converted into EFM.

Channel Bits

One of 14 bits converted from 8 bits is called a channel bit.

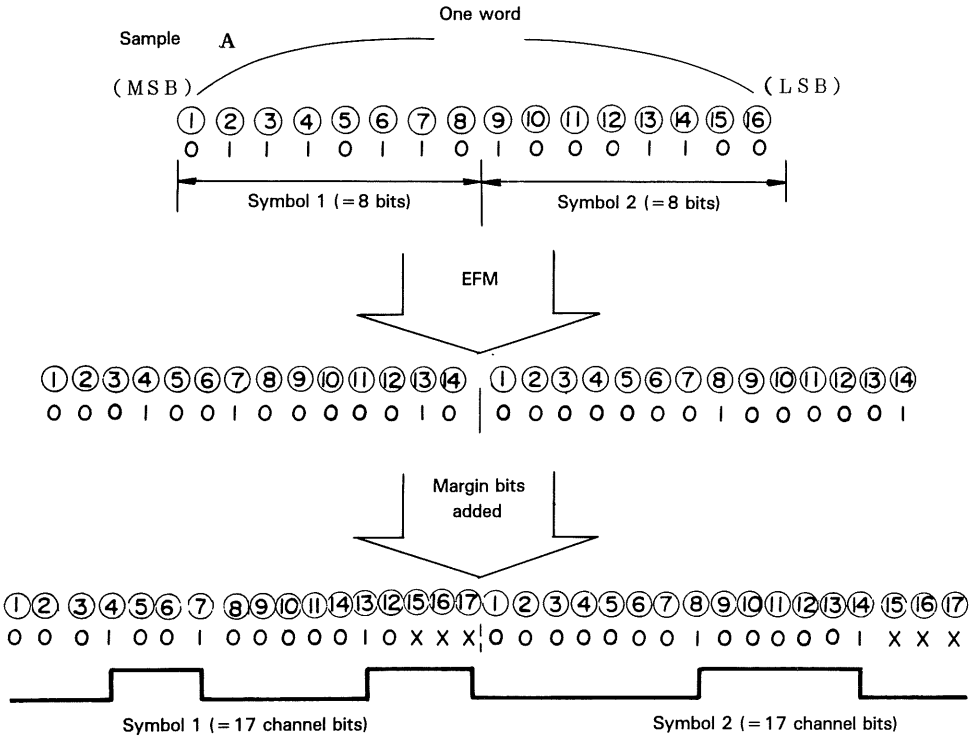


Fig. 1.8

(1) EFM is the modulation to first divide a 16-bit datum (data bit) into two 8-bit data and then convert each of these 8-bit data to a 14-bit datum (channel bit) as shown in Fig. 1.8. The conversion is to select patterns of 2^8 kinds among patterns of 2^{14} kinds, meeting the following condition. Channel bits of 2^8 meeting this condition have been predetermined by a computer as indicated in Tables 1-1 and 1-2:

> Two or more but 10 or less 0s (zeros) should be always inserted between channel bits 1 and 14.

(2) Three channel bits are always inserted between 14-bit blocks. The role of these 3 bits is to make adjustment so that the above condition (enclosed in the box) is met even at the connection of blocks.

II. FUNDAMENTALS

Order	8 bits→14 bits	
	data bits	channel bits
0	00000000	01001000100000
1	00000001	10000100000000
2	00000010	10010000100000
3	00000011	10001000100000
4	00000100	01000100000000
5	00000101	00000100010000
6	00000110	00010000100000
7	00000111	00100100000000
8	00001000	01001001000000
9	00001001	10000001000000
10	00001010	10010001000000
11	00001011	10001001000000
12	00001100	01000001000000
13	00001101	00000001000000
14	00001110	00010001000000
15	00001111	00100001000000
16	00010000	10000000100000
17	00010001	10000010000000
18	00010010	10010010000000
19	00010011	00100000100000
20	00010100	01000010000000
21	00010101	00000010000000
22	00010110	00010010000000
23	00010111	00100010000000
24	00011000	01001000010000
25	00011001	10000000010000
26	00011010	10010000010000
27	00011011	10001000010000
28	00011100	01000000010000
29	00011101	00001000010000
30	00011110	00010000010000
31	00011111	00100000010000
32	00100000	00000000100000
33	00100001	10000100001000
34	00100010	00001000100000
35	00100011	00100100100000
36	00100100	01000100001000
37	00100101	00000100001000
38	00100110	01000000100000
39	00100111	00100100001000
40	00101000	01001001001000
41	00101001	10000001001000
42	00101010	10010001001000
43	00101011	10001001001000
44	00101100	01000001001000
45	00101101	00000001001000
46	00101110	00010001001000
47	00101111	00100001001000
48	00110000	00000100000000
49	00110001	10000010001000
50	00110010	10010010001000
51	00110011	10000100010000
52	00110100	01000100001000
53	00110101	00000010001000
54	00110110	00010010001000
55	00110111	00100010001000
56	00111000	01001000001000
57	00111001	10000000001000
58	00111010	10010000001000
59	00111011	10001000001000
60	00111100	01000000001000
61	00111101	00001000001000
62	00111110	00010000001000
63	00111111	00100000001000

Order	8 bits→14 bits	
	data bits	channel bits
64	01000000	01001000100100
65	01000001	10000100100100
66	01000010	10010000100100
67	01000011	10001000100100
68	01000100	01000100100100
69	01000101	00000000100100
70	01000110	00010000100100
71	01000111	00100100100100
72	01001000	01001001000100
73	01001001	10000001000100
74	01001010	10010001000100
75	01001011	10001001000100
76	01001100	01000001000100
77	01001101	00000001000100
78	01001110	00010001000100
79	01001111	00100001000100
80	01010000	10000000100100
81	01010001	10000010000100
82	01010010	10010010000100
83	01010011	00100000100100
84	01010100	01000010000100
85	01010101	00000010000100
86	01010110	00010010000100
87	01010111	00100010000100
88	01011000	01001000000100
89	01011001	10000000000100
90	01011010	10010000000100
91	01011011	10001000000100
92	01011100	01000000000100
93	01011101	00001000000100
94	01011110	00010000000100
95	01011111	00100000000100
96	01100000	01001000100010
97	01100001	10000100100010
98	01100010	10010000100010
99	01100011	10001000100010
100	01100100	01000100100010
101	01100101	00000000100010
102	01100110	01000000100100
103	01100111	00100100100010
104	01101000	01001001000010
105	01101001	10000001000010
106	01101010	10010001000010
107	01101011	10001001000010
108	01101100	01000001000010
109	01101101	00000001000010
110	01101110	00010001000010
111	01101111	00100001000010
112	01110000	10000000100010
113	01110001	10000010000010
114	01110010	10010010000010
115	01110011	00100000100010
116	01110100	01000010000010
117	01110101	00000010000010
118	01110110	00010010000010
119	01110111	00100010000010
120	01111000	01001000000010
121	01111001	00001001001000
122	01111010	10010000000010
123	01111011	10001000000010
124	01111100	01000000000010
125	01111101	00001000000010
126	01111110	00010000000010
127	01111111	00100000000010

d1.....d8 C1.....C14

C1 is first cut.

EFM Conversion table 0 to 127
(NRZ-1 represantation)

II. FUNDAMENTALS

Order	8 bits→14 bits	
	data bits	channel bits
128	10000000	01001000100001
129	10000001	10000100100001
130	10000010	10010000100001
131	10000011	10001000100001
132	10000100	01000100100001
133	10000101	00000000100001
134	10000110	00010000100001
135	10000111	00100100100001
136	10001000	01001001000001
137	10001001	10000001000001
138	10001010	10010001000001
139	10001011	10001001000001
140	10001100	01000001000001
141	10001101	00000001000001
142	10001110	00010001000001
143	10001111	00100001000001
144	10010000	10000000100001
145	10010001	10000010000001
146	10010010	10010010000001
147	10010011	00100000100001
148	10010100	01000010000001
149	10010101	00000010000001
150	10010110	00010010000001
151	10010111	00100010000001
152	10011000	01001000000001
153	10011001	10000010010000
154	10011010	10010000000001
155	10011011	10001000000001
156	10011100	01000010010000
157	10011101	00001000000001
158	10011110	00010000000001
159	10011111	00100010010000
160	10100000	00001000100001
161	10100001	10000100001001
162	10100010	01000100010000
163	10100011	00000100100001
164	10100100	01000100001001
165	10100101	00000100001001
166	10100110	01000000100001
167	10100111	00100100001001
168	10101000	01001001001001
169	10101001	10000001001001
170	10101010	10010001001001
171	10101011	10001001001001
172	10101100	01000001001001
173	10101101	00000001001001
174	10101110	00010001001001
175	10101111	00100001001001
176	10110000	00000100100000
177	10110001	10000010001001
178	10110010	10010010001001
179	10110011	00100100010000
180	10110100	01000010001001
181	10110101	00000010001001
182	10110110	00010010001001
183	10110111	00100010001001
184	10111000	01001000001001
185	10111001	10000000001001
186	10111010	10010000001001
187	10111011	10001000001001
188	10111100	01000000001001
189	10111101	00001000001001
190	10111110	00010000001001
191	10111111	00100000001001

Order	8 bits→14 bits	
	data bits	channel bits
192	11000000	01000100100000
193	11000001	10000100010001
194	11000010	10010010010000
195	11000011	00001000100100
196	11000100	01000100010001
197	11000101	00000100010001
198	11000110	00010010010000
199	11000111	00100100010001
200	11001000	00001001000001
201	11001001	10000100000001
202	11001010	00001001000100
203	11001011	00001001000000
204	11001100	01000100000001
205	11001101	00000100000001
206	11001110	00000010010000
207	11001111	00100100000001
208	11010000	00000100100100
209	11010001	10000010010001
210	11010010	10010010010001
211	11010011	10000100100000
212	11010100	01000010010001
213	11010101	00000010010001
214	11010110	00010010010001
215	11010111	00100010010001
216	11011000	01001000010001
217	11011001	10000000010001
218	11011010	10010000010001
219	11011011	10001000010001
220	11011100	01000000010001
221	11011101	00001000010001
222	11011110	00010000010001
223	11011111	00100000010001
224	11100000	01000100000010
225	11100001	00000100000010
226	11100010	10000100010010
227	11100011	00100100000010
228	11100100	01000100010010
229	11100101	00000100010010
230	11100110	01000000100010
231	11100111	00100100010010
232	11101000	10000100000010
233	11101001	10000100000100
234	11101010	00001001001001
235	11101011	00001001000010
236	11101100	01000100000100
237	11101101	00000100000100
238	11101110	00010000100010
239	11101111	00100100000100
240	11110000	00000100100010
241	11110001	10000100010010
242	11110010	10010010010010
243	11110011	00001000100010
244	11110100	01000100010010
245	11110101	00000100010010
246	11110110	00010010010010
247	11110111	00100010010010
248	11111000	01001000010010
249	11111001	10000000010010
250	11111010	10010000010010
251	11111011	10001000010010
252	11111100	01000000010010
253	11111101	00001000010010
254	11111110	00010000010010
255	11111111	00100000010010

d1.....d8 C1.....C14

C1 is first cut.

data bits channel bits

EFM Conversion table 128 to 255
(NRZ-1 represantation)

cf: NRZ Non Return to Zero

II. FUNDAMENTALS

1-6 FRAME SYNCHRONIZATION AND FRAME STRUCTURE

Reproduction signals cannot be recovered RF signals do not come out for a long time due to dropout or one information bit has been shifted owing to jittering in digital recording or playback. Because one bit shift of a digital signal makes the signal quite different in its signal level.

Therefore, by dividing a recorded signal to many small blocks, the system is organized so that even when a signal is disturbed due to jittering or the like, a bit synchronization is always estabilished at the new block to identify the joint part between blocks. Such a block is called a "Frame". Frame Sync signals are inserted to indicate the boundary of the frame and to make a bit synchronization. Fig. 1.9 shows the structure of one frame.

	Channel bits	Margin bits	Total bits
Frame Synchronization	24	3	27
Users buts	14	3	17
Data bits	14 bit×24=336	3 bit×8=24=72	408
Error correction bits (Parity bits)	14 bit×8=112	3 bit×24	136
	486	102	588

Frame Structure

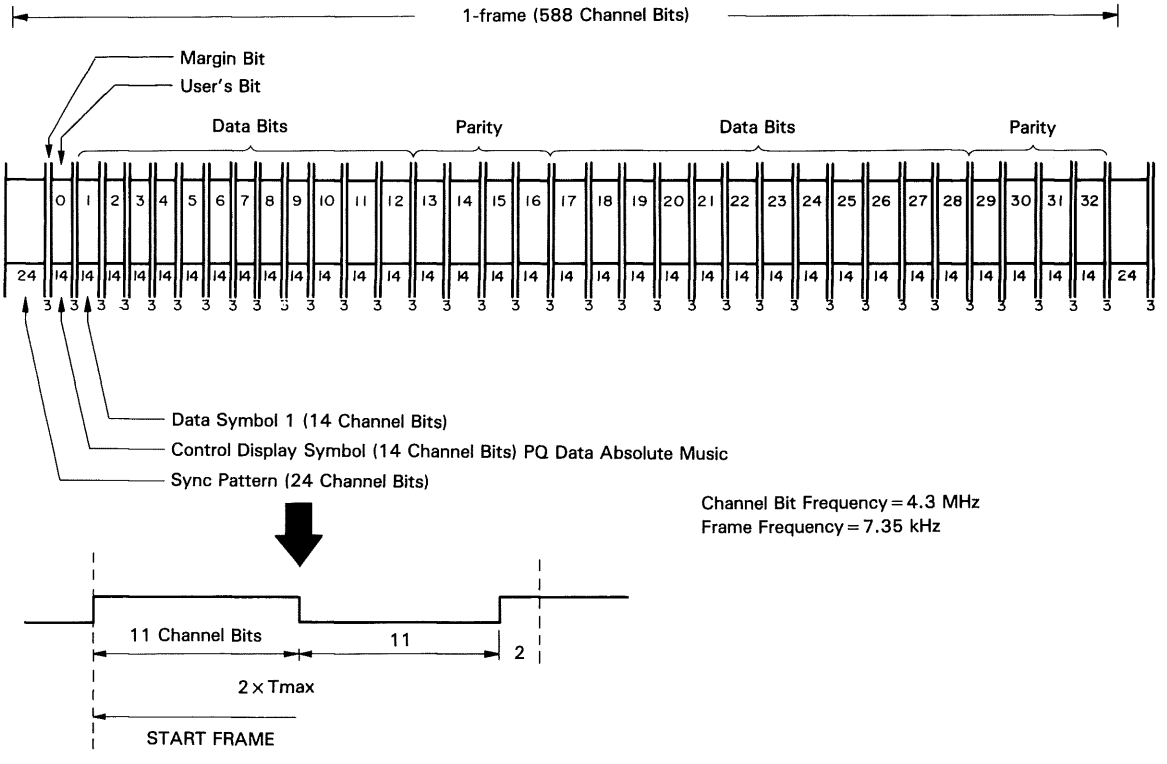


Fig. 1.9

II. FUNDAMENTALS

1-7 COMPACT DISC (CD)

1. There are many kinds of DAD systems: CD, MD and AHD. (Refer to Fig. 1.10)

2. DP-1100B/II adopts the CD system. The CD system is also called "a light system". A light beam from a semiconductor laser is converged with an objective lens to hit pits inside a disc for using their reflected light.

3. There are no groove in the CD system hit pits.
Size of Pit: Width 0.5 μm, Length: 0.9 to 3.3 μm, Depth: 0.1 μm

4. Laser beam is hit through a transparent disc layer to read out data. (See Fig. 1.11)

5. Construction of disc. (See Fig. 1.11)

6. Disc baseplates are usually made of PC (polycarbonate), PMMA (acryl) is superior for a disc baseplate, but its moisture absorption causing bend is a big defect. (Refer to precautions on handling the disc.)

7. Playback time is 60 minutes with a 120 mm disc. Dimensions are given in Fig. 1.12.

8. The rotating speed of the disc is not constant. Because of a constant linear velocity system employed, the rotating speed is varied between around 500 to 200 r.p.m. (counterclockwise) CLV (constant linear velocity): capstan drive type taperecorder CAV (constant angular velocity): rim drive type taperecorder.

9. PU (pickup) does not contact a disc surface but traces a track moving from inner radius to outer radius.

10. How much effectively does it use a laser beam?
It depends upon the transmission factor, reflection factor and double refraction.

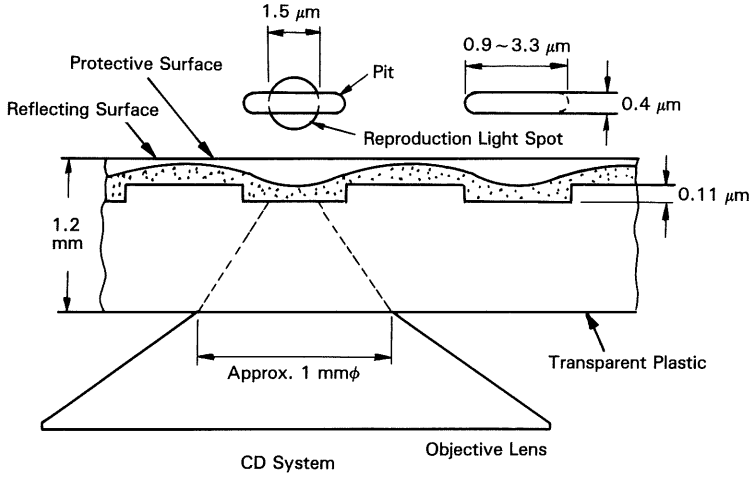


Fig. 1.10

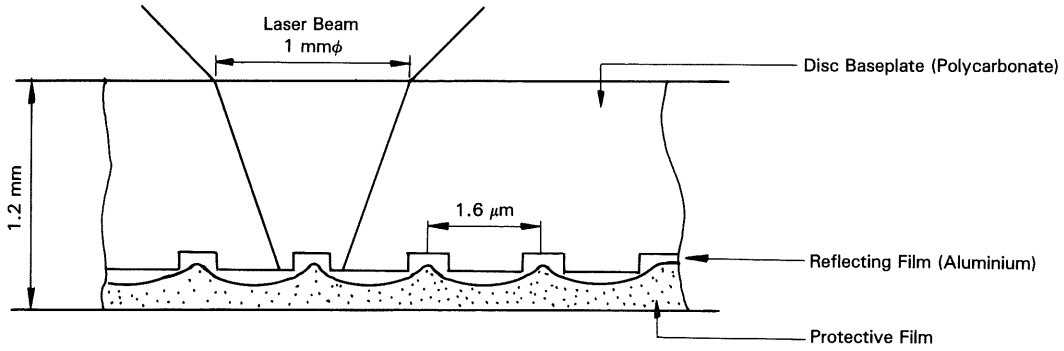


Fig. 1-11

II. FUNDAMENTALS

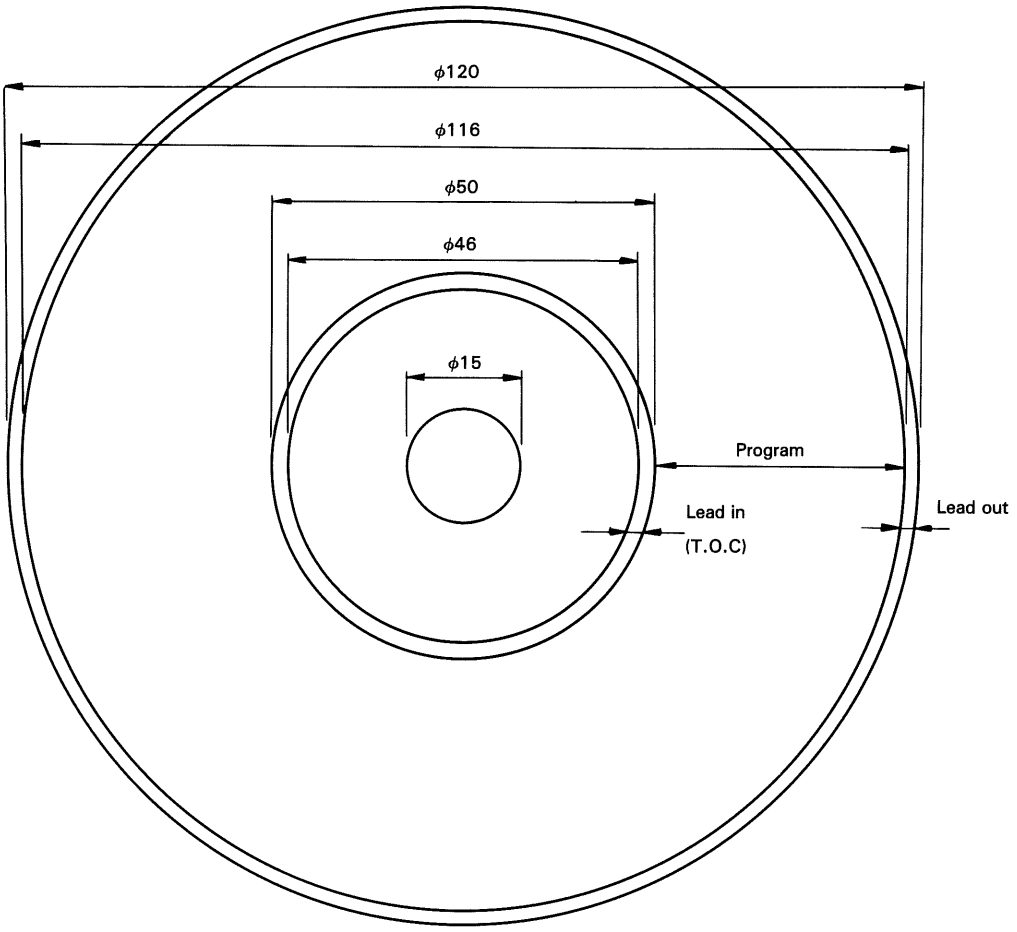


Fig. 1.12

Lead In: TOC (table of contents) → Absolute time of the heading of music is included.
Lead Out: Used for retrieving of the heading indicates of program end.
Other → Control Data P, Q

II. FUNDAMENTALS

11.

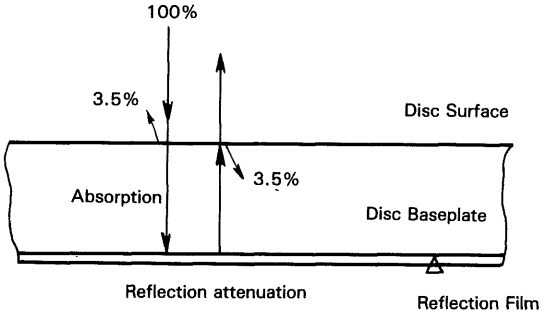


Fig. 1.13

12. Double Refraction
The rating of double refraction is represented by a light path difference (mm). Rating: 100 mm
The main cause of double refraction is mold distortion. Fig. 1.14

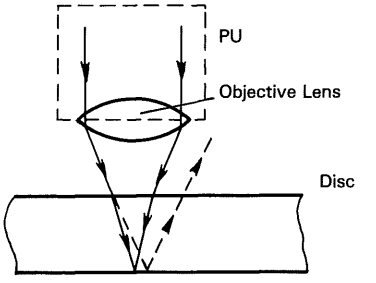
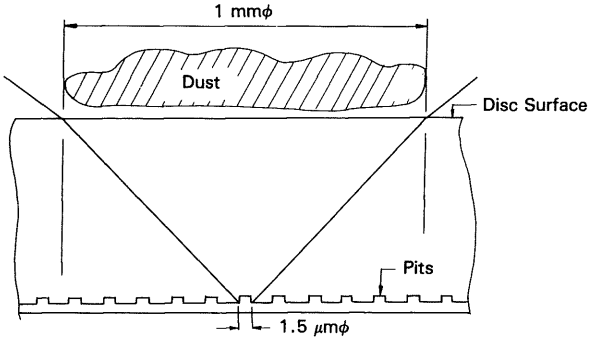
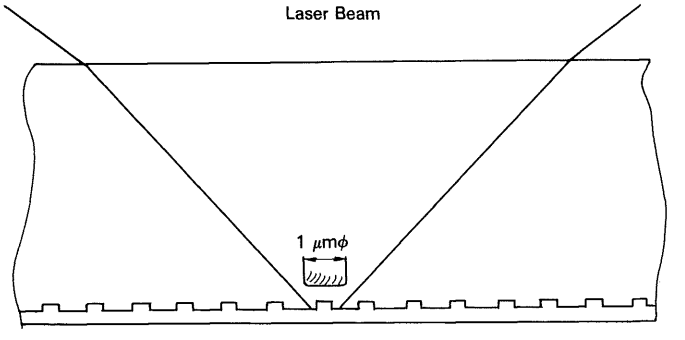


Fig. 1.14

13. CD is tough against dusts Fig. 1.15(a) and (b)



(a) In a case where dusts are deposited on the disc surface



(b) In a case where dusts are attached to a reflecting film surface

Fig. 1.15

14. Fabricating process of baseplate. Fig. 1.16

15. Mastering: Procedures for Photo-resist coating, laser recording and development are included. This is corresponding to the fabricating process of a lacquer disc in an analog record production.

16. Molding: Injection molding
Photo Polymerization

II. FUNDAMENTALS

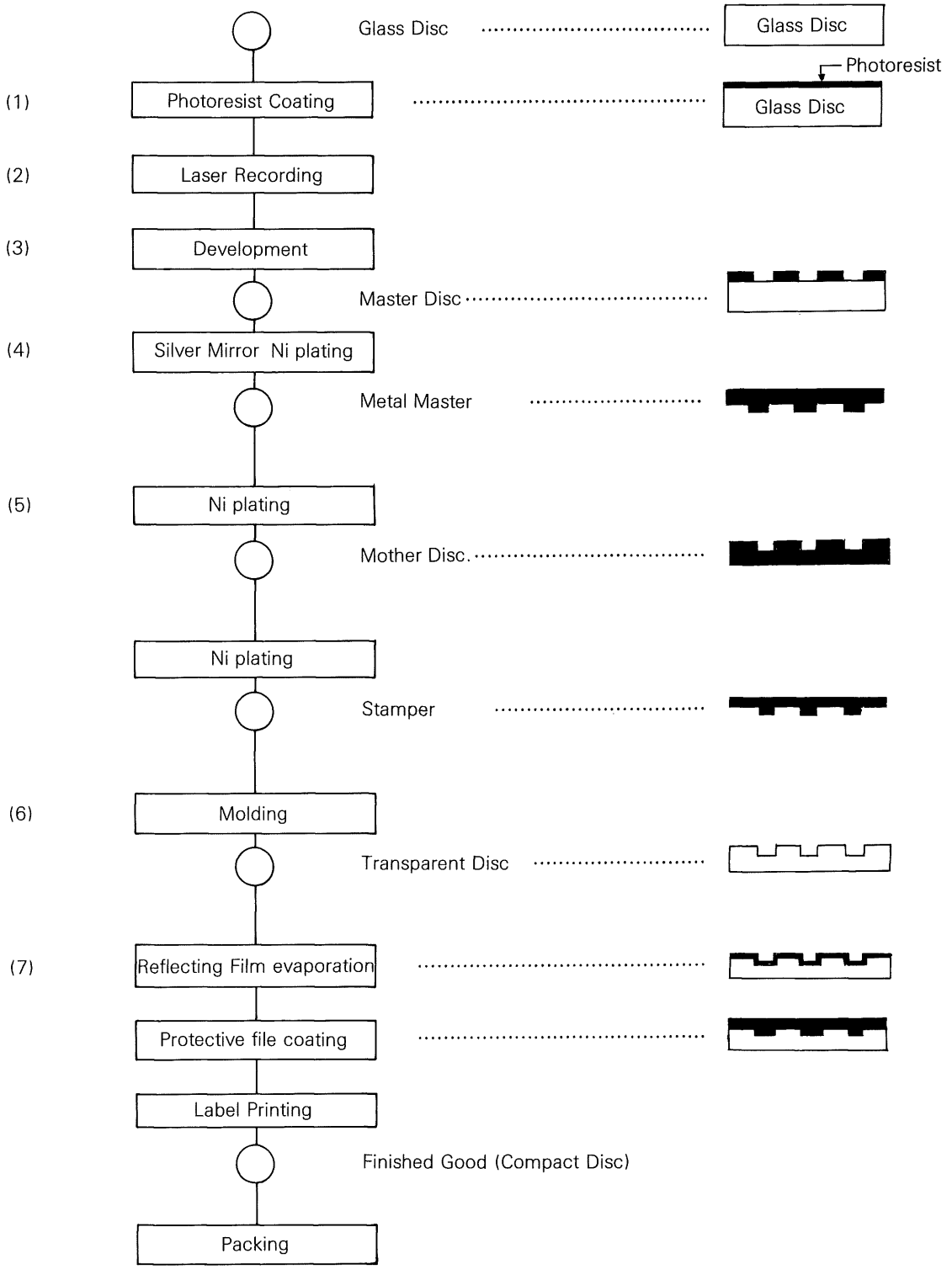


Fig. 1.16 Manufacturing Process of CD

II. FUNDAMENTALS

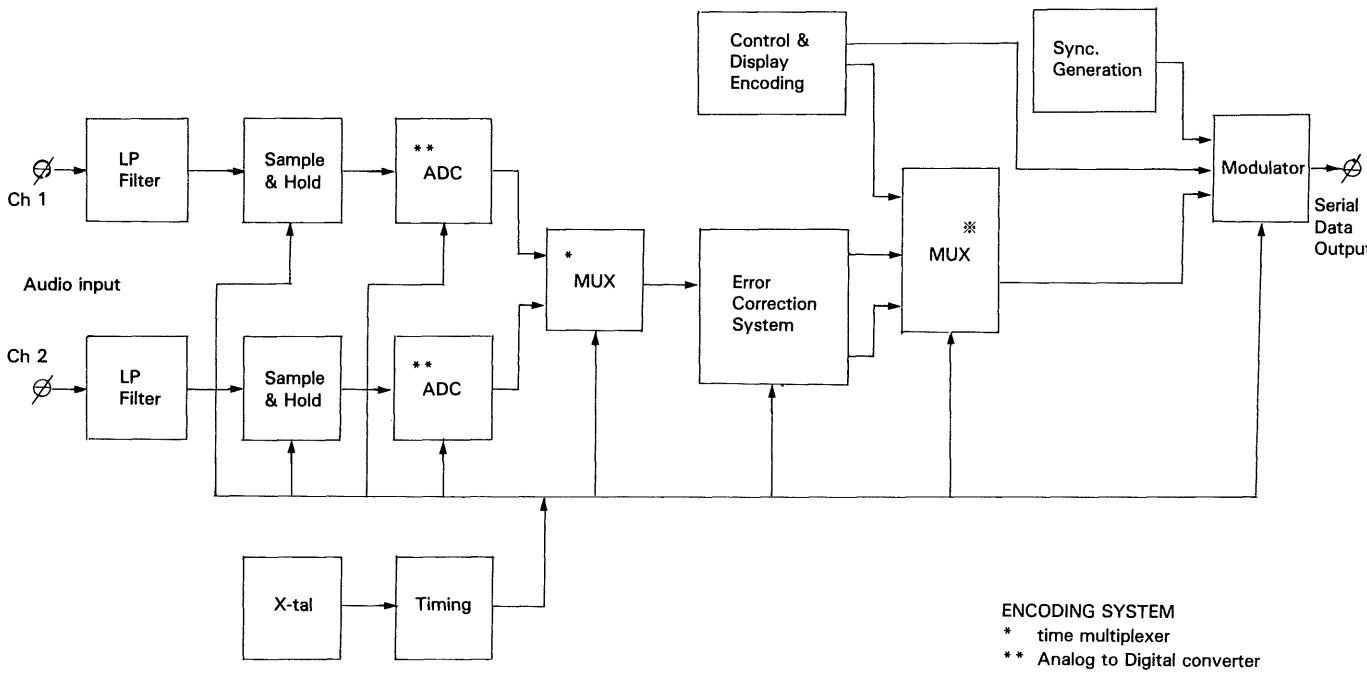


Fig. 1.17 Encoding system

II. FUNDAMENTALS

2 CODE ERROR

2-1 CAUSES OF CODE ERROR

(1) Defectives which are already present on a disc at delivery:
- — Dusts attached to pits during production of disc.
- — Disc molding distortion (entering of air bubbles whose refraction factor is not equal.)

(2) Faults created on handling of a disc: dusts, scratches, stains and finger prints.

(3) Level variations of reproduction signal (eye pattern) Because protection of out-of-tracking, Focus and CLV are all depending on a servo system, poor stability of the servo leads to increased code errors.

2-2 KINDS OF CODE ERROR

(1) Random Error: an error which causes an error in one bit

(2) Burst Error: an error which causes an error in many successive bits.

2-3 INTERLEAVE

Even if reading every page of a book slantwise from its upper left side to lower right side, you can fully recognize the context or contents. However, you cannot recognize the contents of the book if you are reading carefully one character or clause without reading several tens of pages.

An error collection code is the same as this, and correction is easy even when code errors of some bits are present. However, if many, say 1000, bits are consecutively wrong at a time, it is very difficult to correct those errors.

Therefore, the technique with which an order of a signal is once changed and then recorded and, after reproduction, returned back to the original order is employed. This changing of the order of a signal is called an "interleave", and the returning to the original order is called a "deinterleave".

Fig. 2.1 is the illustration explaining the principle of interleave. The order of a signal at fabrication of the disc is out of order. Therefore, by deinterleaving the signal, successive code errors are disperesed, so that operation of error correction and associated jobs are made facilitative.

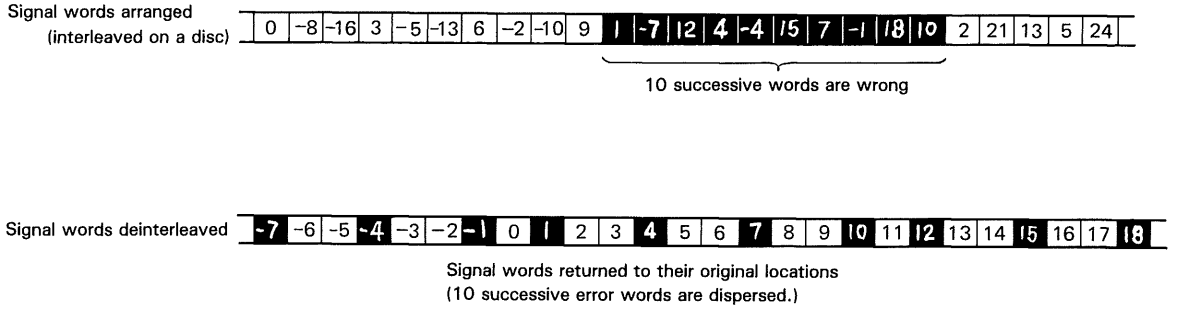


Fig. 2.1

II. FUNDAMENTALS

2-4 SINGLE ERASURE CORRECTING METHOD

(1) Bill (a) as shown in Fig. 2-2 indicates prices of four kinds of articles A, B, C and D and the total. In bill (b), the price of article B disappears. This calls a disappearance or erasure. When the total amount is known, the price of article B can be found even if one figure is missed. In the coding theory, wether the total amount is correct in bill (a) is checked. This operation is called "syndrome".

Bill (a)

	A	¥ 100
	B	¥ 200
	C	¥ 300
+	D	¥ 400
	Total P	¥ 1,000

Syndrome (Checking)
$S = A + B + C + D - P = 0$

(2) In bill (b), the price of article B disappears. (It is indicated by B*. $B^* = 0$) Conducting the syndrome does not creat $S = 0$ because there is an erasure. However, as the number of erasure is one, the amount of B* can be found from syndrome $S = -200$. According to the single diserasure correcting method, operation of correction is conducted on the assumption that all other data (A', C' and D') are correct. If there is an error for another article, miscorrection happens.

Bill (b)

	A'	¥ 100	
	B*	¥ ?	← Disppearance
	C'	¥ 300	
+	D'	¥ 400	
	Total P'	¥ 1,000	

Syndrome (Checking)
$S = A' + B' + C' + D' - P = 0$
$B = B^* - S = 200$

(3) Operating the syndrorme on bill (c), zero does not come out. Therefore, it may be found that something is wrong, but it cannot be found which of A', B', C', D' and P' is incorrect. In such a case, correction is infeasible.

Bill (c)

	A'	¥ 100
	B'	¥ 300
	C'	¥ 300
+	D'	¥ 400
	Total P'	¥ 1,000

$S = A' + B' + C' + D' - P' = 0$

(4) Bill (d) illustrates the example that the location to be corrected is known, and the correction can be done by the same means as in bill (b). The means to indicate the location of error in such a way is called a "pointer".

In the examples of (1) to (4), "Total P" is used for check of error or erasure of data A, B, C and D. A word used for check and correction besides required data is called a "parity word" or a "parity bit".

Bill (d)

	A'	¥ 100
	B*	¥ 300
	C'	¥ 300
+	D'	¥ 400
	Total P'	¥ 1,000

$S = A' + B' + C' + D' - P' = 100$
$B = B^* - S = 200$

II. FUNDAMENTALS

2-5 SINGLE ERROR CORRECTION, DOUBLE ERASURES

(1) In case of (3) in 2-4, correction is infeasible because the location of error is unknown. Even in such a case, the way by which correction is feasible is a single error correcting method. In 2-4, there is only one parity word, P. Besides this, a "Weighted Total Value", Q, is used. Because two parity words P and Q are used, there are also two syndromes S_1 And S_2.

Now suppose that there is an incorrect bill (b) in respect to a correct bill (b) and that the location of error (one) in bill (b) is unknown.

Supposing that the differences from original values are E_A, E_B, E_C, E_D, E_P and E_Q with respect to A', B', C', D', P' and Q', respectively, of bill (b) (for no error, E_A, to $E_Q = 0$)
$A' = A + E_A$, $B' = B + E_B$, $C' = C + E_C$, $D' = D + E_D$, $P' = P + E_D$, $Q' = Q + E_Q$

Obtaining syndrome S_1,

$$S_1 = A' + B' + C' + D' - P'$$
$$= (A + E_A) + (B + E_B) + (C + E_C) + (D + E_D) - (P + E_P)$$
$$= A + B + C + D - P + E_A + E_B + E_C + E_D - E_P - E_P - (1)$$
$$0$$
$$= E_A + E_B + E_C + E_D - E_P$$

Obtaining syndrome S_2

$$S_2 = 4A' + 3B' + 2C' + D' - Q'$$
$$= 4A + 3B + 2C + D - Q + (4E_A + 3E_E + 2E_C + E_D - E_Q) \quad (2)$$
$$0$$
$$= 4E_A + 3E_B + 2E_C + E_D - E_Q$$

Supposing that a code error is one word between A' to P', Q'

(I)	A' wrong	$S_1 = E_A$, $S_2 = 4E_A$
(II)	B' wrong	$S_1 = E_B$, $S_2 = 3E_B$
(III)	C' wrong	$S_1 = E_C$, $S_2 = 2E_C$
(IV)	D' wrong	$S_1 = E_D$, $S_2 = E_D$
(VI)	P' wrong	$S_1 = E_P$, $S_2 = 0$
(VII)	Q' wrong	$S_1 = 0$, $S_2 = -E_Q$

By a method where two syndromes are introduced as mentioned above and determined, wrong words can be found and corrected.

Bill (a)

A	¥ 100
B	¥ 200
C	¥ 300
D	¥ 400
P	¥ 1,000
Q	¥ 1,000

$P = A + B + C + D$
$Q = 4A + 3B + 2C + D$

Syndromes
$S_1 = A + B + C + D - P = 0$
$S_2 = 4A + 3B + 2C + D - Q = 0$

Bill (b)

A'	¥ 100
B'	¥ 300
C'	¥ 300
D'	¥ 400
P'	¥ 1,000
Q'	¥ 2,000

Syndrome
$S_1 = A' + B' + C' + D' - P' = 100$
$S_2 = 4A' + 3B' + 2C' + D' - Q' = 300$

II. FUNDAMENTALS

(2) The principle of double erasure correction is described below. In this case, the location of error is indicated with a pointer. It is here known that two words in bill (c) are wrong and there are no other wrong words.
Using equation (1) in paragraph (1),

$$S_1 = A + B + C + D - P + E_A + E_B + E_C + E_D - E_P = 200$$
$$0$$

Supposing $E_A = 0$, $E_D = 0$ and $E_P = 0$

$$S_1 = E_B + E_C = 200 \quad \text{(3)}$$

From Equation (2) of (1)

$$S_2 = 4A + 3B + 2C + D + (4E_A + 3E_B + 2E_C + E_D - E_Q) = 500$$
$$0$$

$$S_2 = 3E_B + 2E_C = 500 \quad \text{(4)}$$

Determining E_B and E_C from simultaneous equations of (3) and (4),

EB = 100

Bill (c)		
A'	¥	100
B'	¥	300
C'	¥	400
D'	¥	400
P'	¥	1,000
Q'	¥	2,000

Pointer

$E_C = 100$

$S_1 = A' + B^* + C^* + D' - P' = 200$
$S_2 = 4A' + 3B' + 2C^* + D' - Q' = 500$
Where
$B^* = E + E_B$ $C^* + = C + E_C$

This theory is the principle of a Reed Solomon Code. In practice, the Reed Solomon Code with four parity words is used.

II. FUNDAMENTALS

2-6 CROSS-INTERLEAVE

(1) Fig. 2.2 shows a principle of a cross-interleave. An original series of signals is divided into a number of words, and parity words are inserted.

$$\begin{aligned} P_1 &= W_1 + W_2 + W_3 + W_4 \\ P_5 &= W_5 + W_6 + W_7 + W_8 \\ P_9 &= W_9 + W_{10} + W_{11} + W_{12} \end{aligned} \quad (5)$$

Four original series of signals (W_1, W_5, W_9, W_{13}...), (W_2, W_6, W_{10}, W_{14},...), (W_3, W_7, W_{11}, W_{15},...) and (W_4, W_8, W_{12}, W_{16},...) among many original series of signals are arranged for four lines No. 1 via No. 4 in Fig. 2.2 of these words, the words passing through No. 1 are delivered directly, but words fed into No. 2 to No. 4 lines are subject to delay with delay memories by one to three words so that the word order is changed (interleaved) at their respective terminals.

There is an adder following the delay memories, where another parity word Q is created.

$$\begin{aligned} Q_1 &= W_1 + W_{-2} + W_{-5} + W_{-8} + W_{-15} \\ Q_5 &= W_5 + W_2 + W_{-1} + W_{-4} + P_{-11} \\ Q_9 &= W_9 + W_6 + W_3 + W_0 + P_{-7} \end{aligned} \quad (6)$$

In other words, two system of codes are used on both sides of the delay memories.

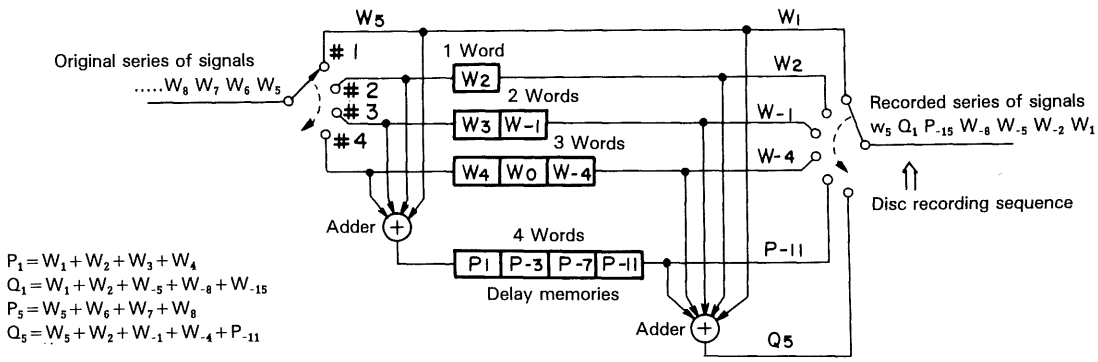


Fig. 2.2 Principle of Cross-Interleave Encoder

(2) Fig. 2.3 indicates relations between two parity codes. The solid lines mean a P's series, and the dotted lines mean a Q's series. Each of them has the capability of single erasure correction, so that an error of a single word can be easily corrected of course.

> The syndrome of each other's series can be used as a pointer for pointing out a location of error.

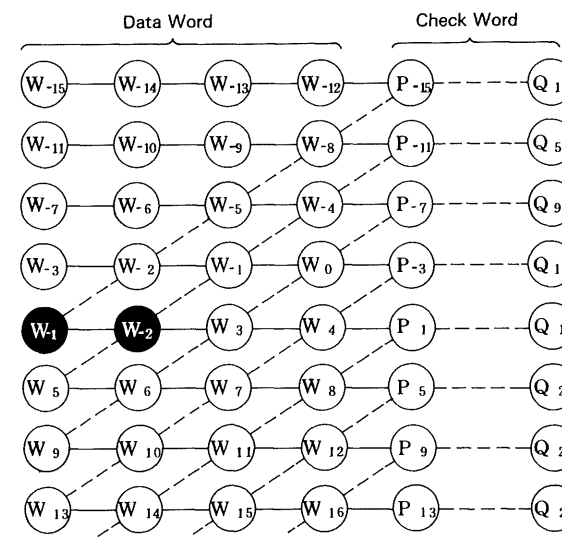


Fig. 2.3 Code Series of Cross Interleave (Black circules indicate errors).

II. FUNDAMENTALS

3 BRIEF EXPLANATIONS ON CD PLAYER (See the BLOCK DIAGRAM)

3-1 PICKUP FOR CD APPLICATION

A pickup part corresponding to a cartridge for a conventional analog player is detailed later. Briefly speaking, this part allows the laser diode to emit a light beam ($\lambda = 780$ nm) and convert the intensity of the reflected light from disc pits into electric signals.

3-2 SIGNAL PROCESSING CIRCUIT

A signal detected at a pickup is delivered to a signal processing circuit, and split into the following three signals.

(1) Focus Error Signal

(2) tracking (Radial) Error Signal

(3) Radio Frequency (RF) Signal: This signal is processed to generate an analog signal.

3-3 SERVO CIRCUIT

3-3-1 Focus Servo Circuit

A focus error signal is fed into a focus servo circuit to control a lens system with the use of a focus servo coil (like a voice coil of a loudspeaker) so that the focus spot of the laser beam is always kept on a pit surface against fluctuations due to the revolutions of a disc. (The same as auto-focusing in an EE camera)

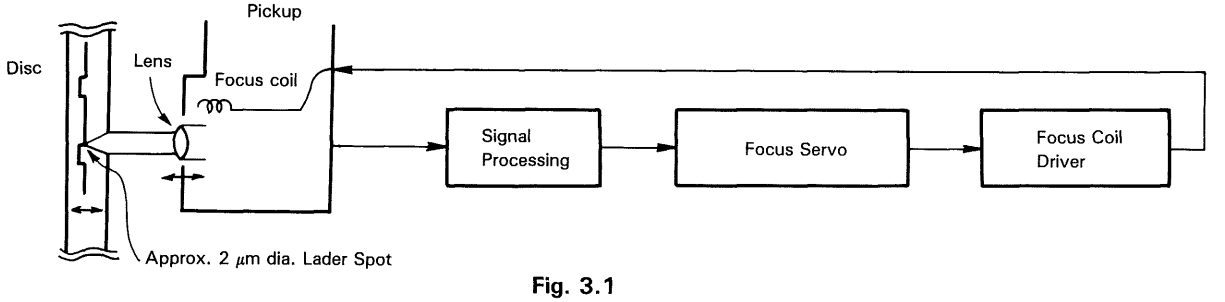


Fig. 3.1

3-3-2 Tracking Servo Circuit

Because a compact disc has no guide groove, it is needed to operate a servo so that a laser beam spot can automaitcally follow a signal track. A tracking error signal is fed into a tracking servo circuit, the output of which drives a tracking servo coil to operate the servo system.

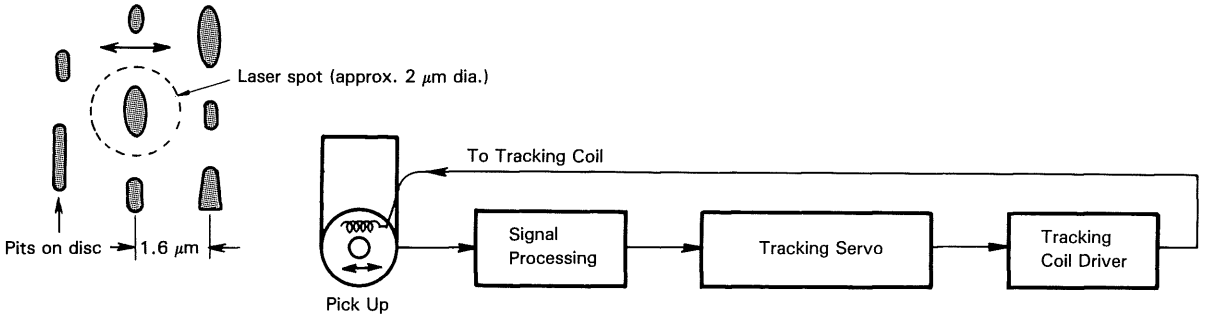


Fig. 3.2

II. FUNDAMENTALS

3-3-3 CLV Servo Circuit

Constant linear velocity (CLV) means to keep a line speed at a constant speed of approx. 1.2 m/sec.
For this purpose disc is rotated: approx. 500 r.p.m. at inside radios
approx. 200 r.p.m. at outside radios

The CLV servo circuit is the circuit to servo-control revolutions of the disc motor to keep circumferential speed of the disc constant.

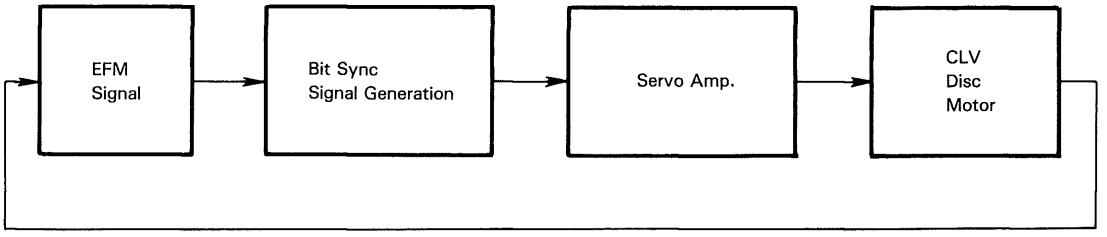


Fig. 3.3

3-4 EYE PATTERN

The RF signal is being delivered from the signal processing circuit as described under **3-2.** The RF signal is vaired acording to appearance or disappearance of a pit on a disc. This signal can be displayed on an oscilloscope as illustrated in the Fig. 3-5.

The waveform is generally called "Eye Pattern".

Fig. 3-5 is sketches explaining concept of the eye pattern. The RF signal is converted to a digital signal composed of 1s and 0s with the aid of a comparator to generate an EFM signal.

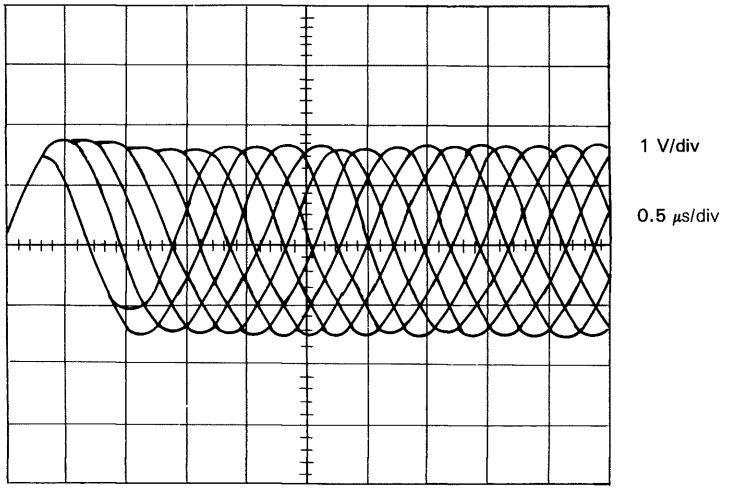


Fig. 3.5

II. FUNDAMENTALS

4 SEMICONDUCTOR LASER (LASER DIODE)

4-1 PRINCIPLE OF LED LIMINESCENCE

A LED is formed with a P-N junction composed of an n-type semiconductor which allows electric conduction with electrons and p-type semiconductor in which holes serves electric conduction. Applying a voltage in the forward direction, electrons in the n-type semiconductor are injected into the p-type semiconductor, and holes in the p- type semiconductor are injected into the n-type semiconductor. Red luminescence is emitted when electrons injected into the p-type semiconductor combine with holes.
Green luminescence is emitted when holes injected into the n-type semiconductor combine with electrons.

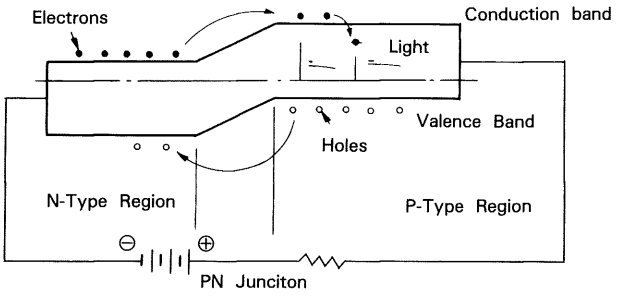


Fig. 4.1

4-2 LASER DIODE

A laser diode, as mentioned **4-1**, is the same as an LED in terms of recombination luminescence of carriers, but different in that the light emitted is a coherent laser light, the phase of which is uniform (single wavelength).

4-3 PROPERTIES REQUIRED FOR A LASER DIODE

(1) Oscillation Wavelength
According to a CD's proposal, there should be the following relaiton between a wavelength of a laser diode and the number of aperture of lens NA:
$\lambda/NA = 1.75\ \mu m$

As long as today's GaAlAs material is used, it is difficult to make a laser diode having a wavelength shorter than apporx. 760 nm, but a laser diode with higher than 780 nm can be made in mass production.

Therefore, $NA = \lambda/1.75\ \mu m = 0.446$

As the result, the objective lens in the pickup used in DP-1100B/II has been designed for approx.
$NA = 0.47 \pm 0.01$

(2) Operating Current
An laser diode has a threshold current I_t with which oscillation starts, and with a current larger than this threshold level, a light power P increases linearly with increase of a current I. Furthermore, if keeping drive at a fixed current, the light outpout is greatly varied due to temperature increase. Therefore, control is always done so that the light output is kept constant.

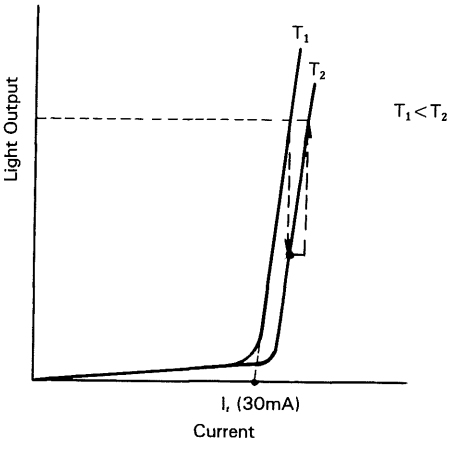


Fig. 4.2 Oscillating Characteristic of a Laser Diode

II. FUNDAMENTALS

5 PICK-UP (PU) AND PU SERVO

5-1 STRUCTURE OF A PICKUP

Light beams emitted from a semiconductor laser are changed to parallel light ralys by a collimator lens system and enter a polarization prism. Since the semiconductor laser beams are linear-polarized in the direction vertical to the plane of incidence, the beams are reflected by the polarizing film. The light beams reflected from another plane of the polarization prism pass through a quarter-wave plate, and then are converged to a spot of nearly 1.5 μm in diameter with the aid of an objective lens.

The light reflected from a disc passes again through the objective lens and follows the same path as the forward path to the polarizing film. By the effect of the quarter-wave plate, the light incoming into the polarizing film is changed so that its polarizing direction is perpendicular to the polarizing direction in the forward path. Therefore, the light transmits the polarizing film and does not go back to the semiconductor laser. Next, the light incoming into a critical angle prism for detection of a foucs point is reflected three times inside the prism and then fed into 4-divided photodiodes. The output of these photodiodes are used for controling a tracking servo coil and a focus servo coil to obtain an optimum focusing of the abjective lens on pits of the disc.

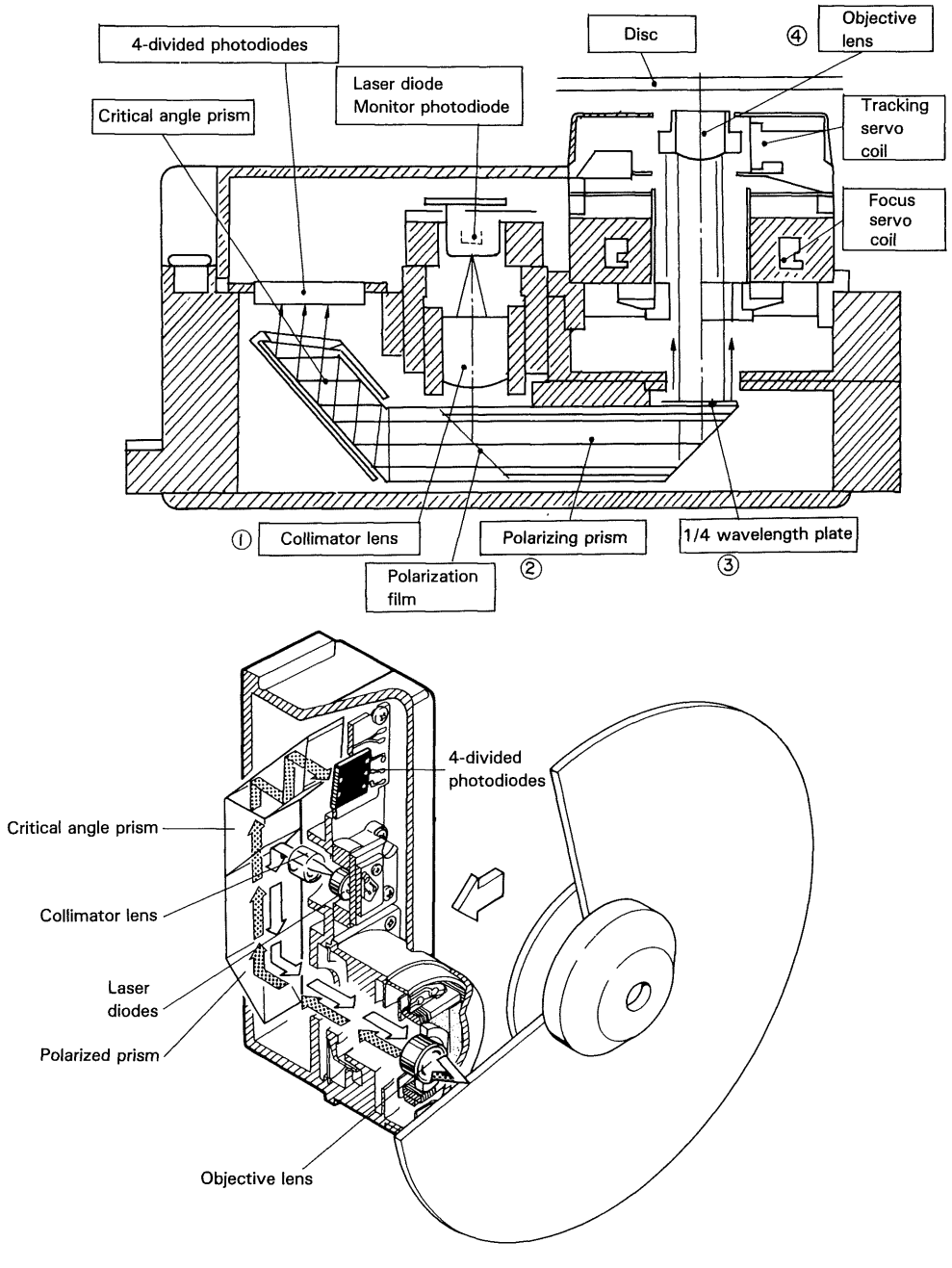


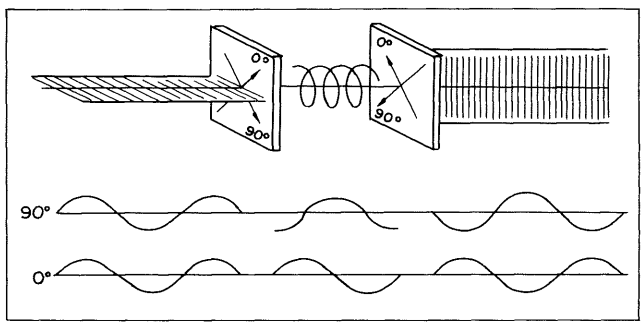
Fig. 5.1

II. FUNDAMENTALS

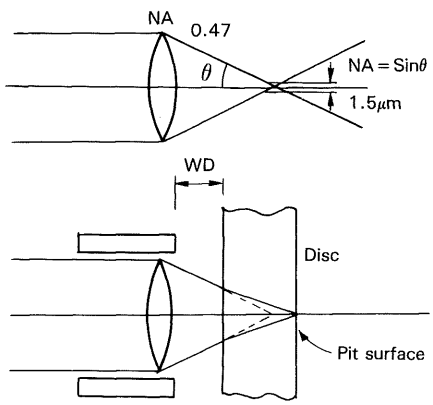
(1) Collimator Lens
Diffused light beams are changed to parallel light beams. Light beams distributed in oval pattern is changed to approx. circular distributions.

(2) Polarized Prism
Light polarized in parallel to a surface is reflected, and light polarized in vertical is passed through the prism.

(3) 1/4 Wavelength Plate



(4) Objective Lens



(5) 4-divided photodiodes
Converts light into an electrical signal.

5-2 FOCUS ERROR AND TRACKING ERROR

To read tiny pits (width: 0.5μm, length 0.9#3.2 μm) on a disc by means of a laser spot, the location must be precisely controlled to follow surface and axial deviations of the disc caused by rotating the disc for playback. For this purpose,

(1) Focus error and
(2) Tracking error

must be detected. The detection muthods for both errors will be given below.

5-2-1 Focus Error Detection

When a light beam is passed from a high refraction material to a low refraction material, a relaion, as shown in Fig. 5.2, is existed between the incident angle and refleciton ratio at the boundary of the materials. As can be seen from the graphs, the reflection ratio will change rapidly as the incident light angle changes in the area where the incident angle is slightly less than the critical angle.

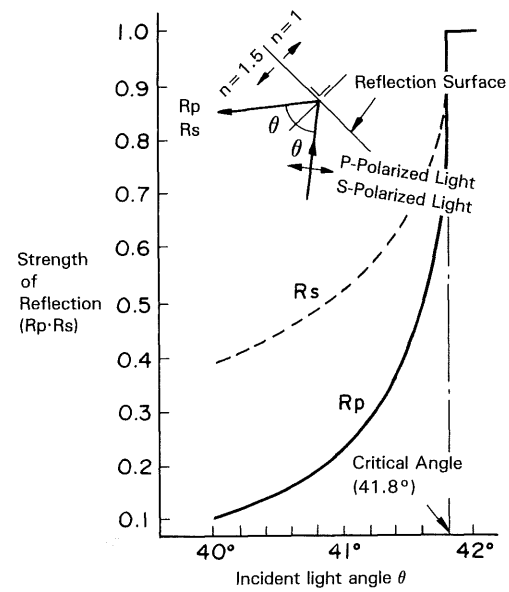
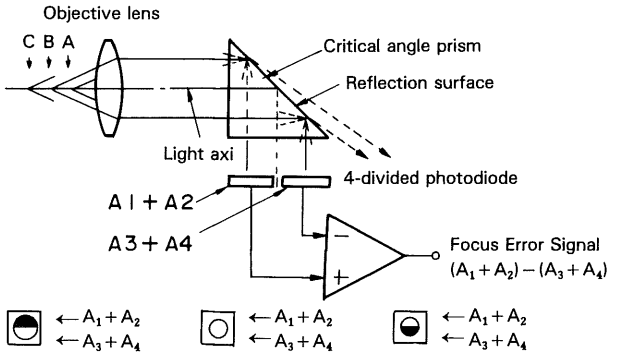


Fig. 5.2 Refleciton changes rapidly at angles dose to critical angle.

II. FUNDAMENTALS

In Fig. 5.3, the angle of the critical prism has been adjusted so that the incident light angle is just equal to the critical angle for a center light beam of incident light. Accordingly, if parallel light beams are impinged, the incident light angle is equal to critical angle for all light beams and all light beams are reflected, giving equal light amount to each element of 4-divided photo-diodes (PDa, PDb, PDc and PDd). If diffused or divergent light is impinged, reflection strength at a left half of the prism lowers and light amount received by the photo diodes PDa and PDb will be decreased. On the contrary, if convergent light is impinged, light amount received by PDc and PDd is reduced. By utilizing this phenomenon, the photo diodes convert light received into four electrical signals and the signals are processed with a differential amplifier to provide a focus error signal in terms of $(A_1+A_2)-(A_3+A_4)$.

(A_1, A_2, A_3, and A_4 Are electrical signals developed by PDa, PDb, PDc and PDd, respectively.)



θc: Criticl angle
−: Disc too close (point A) (divergent light beams....)
●: Focus point (point B) (parallel light....)
+: Disc too far (point C) (convergent light beams....)

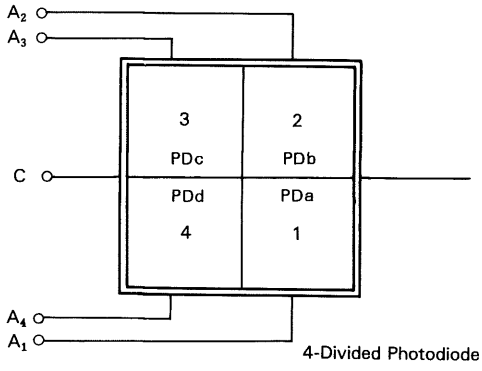
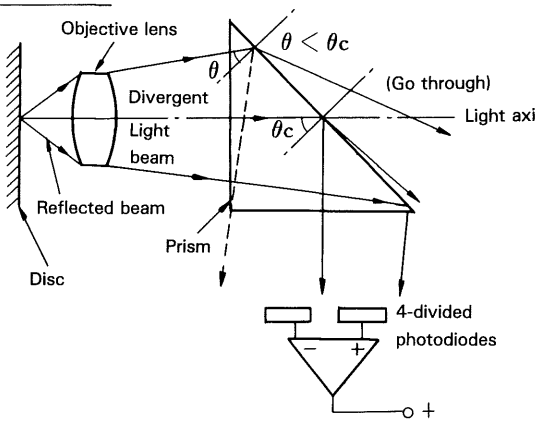
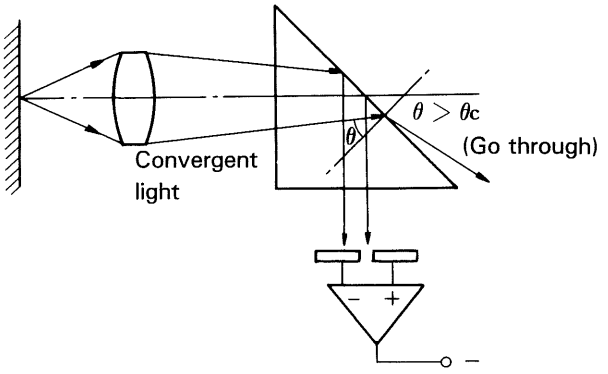


Fig. 5.3 Focus error detection by using a critical prism

Disc too close



Disc Focused



Disc too far

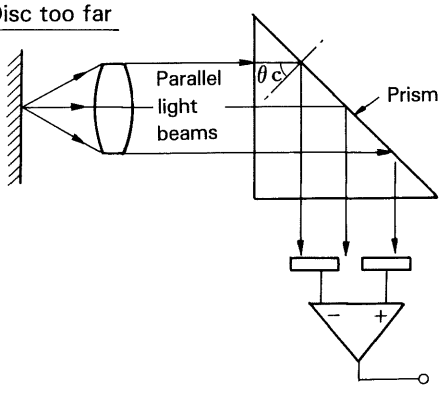


Fig. 5.4 Focus error detection method using a critical angla prism

II. FUNDAMENTALS

5-2-2 Tracking Error Detection

Tracking error is a deviation of the reading light spot from the pits (track) to be traced.

In the Pickup a method called "heterodyne system" is adopted to detect the spot deviation from a pit.

The heterodyne system is based upon the distribution of the reflected light diffracted from a pit depends upon a relative location of the pit and spot.

In this system, each electrical signal converted by the 4-divided photodiode is assumed as A_1, A_2, A_3 And A_4, and A_1+A_3 and A_2+A Are evaluated. Namely, both phases for A_1+A_3 and A_2+A_4 are the same when the tracking is established, while phase difference will be caused when the spot deviates from a pit.

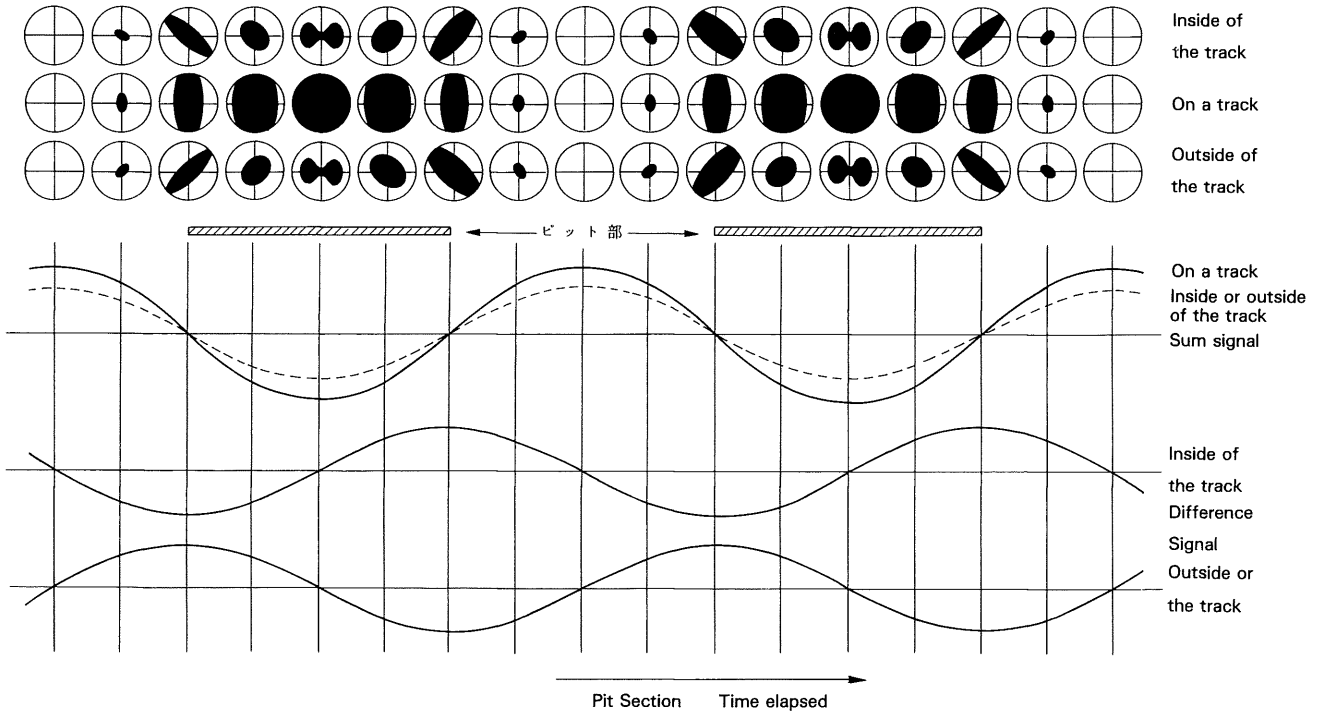


Fig. 5.5 PICKUP Radial Signal Sampling Theory (Pit depth λ/4)

5-3 RF SIGNAL

A RF signal is a sum of each electrical signal A_1, A_2, A_3 and A_4 developed by the 4-divided photodiode (refer to 3-5). The RF signal is then processed to provide EFM signal. The EFM signal is then converted into an analog signal in passing through a D-A convertor after demodulated.

5-4 LIGHT EMISSION FROM LASER DIODE

When the LDC goes H, the output of TA75458(Q108) becomes positive as shown in the schematic diagram, And a current flowing through R145, D102, And D104 turns Q109 cut off, thereby stops the oscillation of the Laser Diode.

When the LDC goes to L level, the output of TA75458 (1/2) changes to negative, and this allows bias current of Q109 to flow from its emitter to the base, thus Q109 is turned on and the Laser diode emits infrared light (810 mm).

When light emitted from the laser diode is impinged to the pin diode, a current proportional to strength of the light flows from anode to cathode of the diode. With the strength of the light increased, a voltage developed across R113 also increases and makes non-inverted (+) terminal of the operational amplifier positive. As the result, the operational amplifier output also increases in positive, thus reducing the current flowing into the laser diode.

II. FUNDAMENTALS

6. GENERAL DESCRIPTION ON MICROPROCESSOR

6-1 Address Data (Q Signal)

1) Address Data (Q Signal) Reading Section
In the CD system specifications, one symbol consisting of 8 bits and located after frame synchronization signal of PCM data is called CONTROL & DISPLAY SYMBOL, and each of 8 bits is called P-Channel, Q-Channel, R-Channel....& W-Channel. Of the eight channels, Q-Channel is used for address data and one address data is comprized of 98 frame Q-Channel data. Fig. 5.6 shows this configuration of the CONTROL & DISPLAY symbol data.

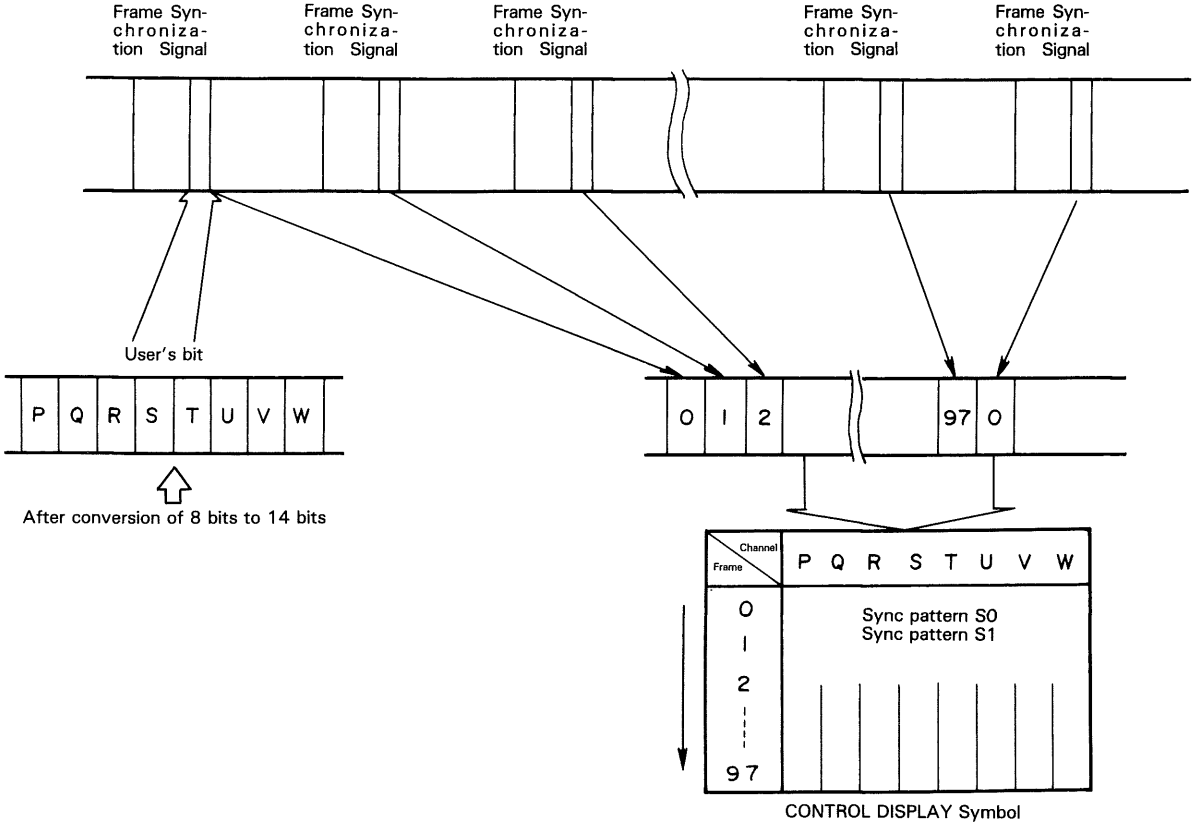
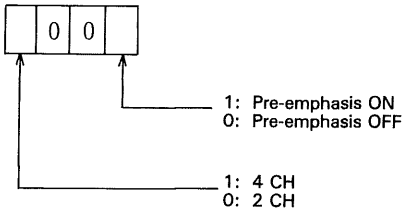


Fig. 6-1

II. FUNDAMENTALS

Address data format (outside lead-in area) are as follows:

SO, S1: 2 bits address signal sync pattern.
CONTROL: 4 bits control data, MSB indicates pre-emphasis on or off, and LSB indicates 4CH/2CH.



ADR: 4 bit mode data
MODE 1 (1 in BCD): Adress mode
MODE 2 (2 in BCD): Disc catalog number mode
MODE 3 (3 in BCD): Special information mode (recorded by alphanumeric code 0#9, A#Z)
MNR: Program number expressed by BCD in 2 digits (8 bits)
X: Index for each program expressed by BCD in 2 digits (8 bits)
MIN: Elapsed time (minute) for each program expressed by BCD in 2 digits (8 bits)
FRAME: Elapsed time for each program expressed by BCD in 2 digits (8 gits) (Frame, 1 frame = 1/75 sec)
ZERO: Not used (8 bits ϕdata)
A MIN: Elapsed time (sec) for disc expressed by BCD in 2 digits (8 bits)
A SEC: Elapsed time (sec) for a disc expressed by BCD in 2 digits (8 bits)
A FRAME: Elapsed time for a disc expressed by BCD in 2 digits (8 bits) (frame).
CRC: 16 bit CRC code data calculated for data CONTROL#A FRAME.

Fig. 6-2 Shows the address data configuration.

Each figure under a code shows bit number required for the code.

S_0, S_1	CONTROL	A D R	M N R	X	M I N	S E C	FRAME	ZERO	AMIN	ASEC	AFRAME	C R C	S_0, S_1
2	4	4	8	8	8	8	8	8	8	8	8	16	

Fig. 6-2 Address Data configuration

1. CIRCUIT DESCRIPTION

Subsequent to "1-2 Head amp", the servo PCB and the process PCB are described in order along the RF signal flow.

1-1 Head amplifier

The four signals from the pickup are input to preamplifier IC (Q103) on the mechanism PCB.

1-1-1 Focus balance and SVC operation circuit (Q103)

The internal block diagram of Q103 is shown in section 2-1-1. Through the resistors, connected between pins 1 and 2 and between pins 15 and 16 of Q103 (TA7731P), focus balance and SVC operation (described later) are performed. Weak signal is amplified and output to servo PCB as S1 and S2.

1-1-2 Focus error signal generation circuit (Q101 and Q104)

The FE amplifier and peak detector, consisting of Q101 and Q104, is a circuit to generate the focus error signal. Peak detection is made with the B-E diode characteristic of Q104 and the CR time constant of its emitter. The focus error signal is obtained from (C + D) - (A + B) operation of the picked-up four signals from the pickup by Q101.

1-1-3 SVC circuit operation (Q102)

The servo control (SVC) is performed by processor IC12 on the process PCB (X32-1010), when the disc is exchanged or when play mode is entered from stop mode. It checks the number of data errors to control control inputs A, B, C and INH of Q102 on the mechanism PCB to obtain the optimum playback.

The internal block diagram and truth table of Q102 is shown in Fig 2-1 C and D of section 2-1-2. Inputs A, B, C and INH, determine which output 0 to 7 (bilateral switch should be internally connected with COM).

1-1-4 APC (laser power control) circuit (Q105, Q106 and Q107)

Q105, which is the laser ON/OFF switch, turns ON with "L" signal LDC (J8-3P) from the microprocessor so that the laser diode emits light. This laser diode incorporates a light emission monitor diode. Then, APC operation is performed by using the monitor output as the APC control input.

1-1-5 FG amplifier circuit (Q101 (2/2), Q108 and Q109)

FG signal is produced by Q101, Q108 and Q109 to monitor the rotation of the disc motor. Q101 performs amplification and Q108, Q109 and D104 perform waveform shaping. For adjustment of each trimming potentiometer, refer to "Adjustment" on page 165.

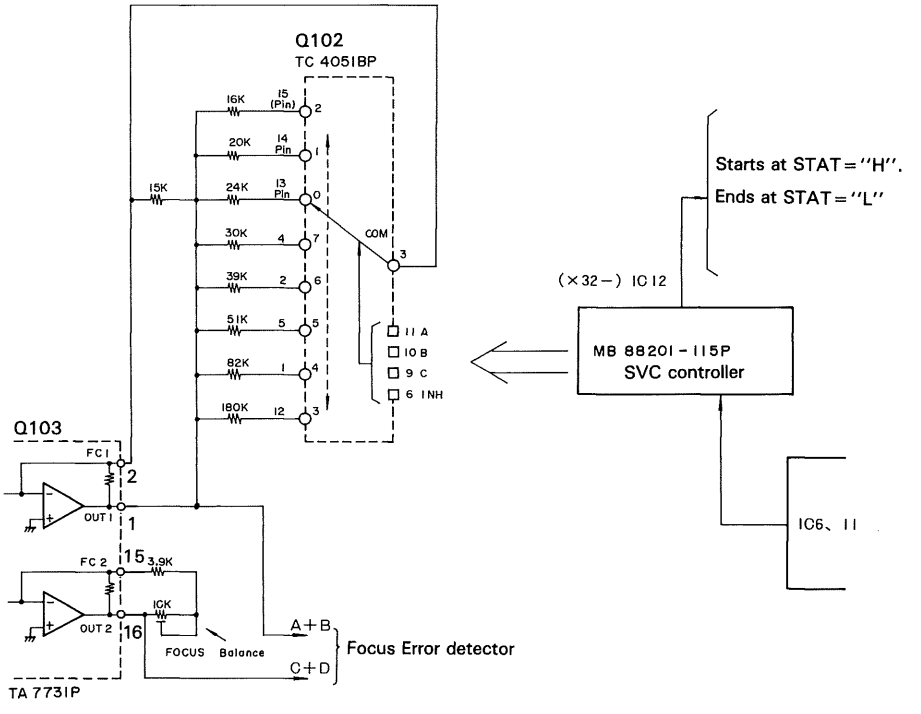


Fig. 1-1-3 SVC Circuit Operation

1. CIRCUIT DESCRIPTION

1-2 Servo circuits

1-2-1 Focus servo circuit

The focus error (FE) signal, generated in the mechanism PCB, is fed into pin 8 of CN6 on the servo PCB. This signal is used in making signal DOK which the presence or absence of the disc is judged when the tray is closed.

With a disc present, "L" signal DOK is output from pin 1 of CN2 to pin 27 of IC15 on the process PCB (X32).

On the other hand, when the RF signal from the pickup is input to pin 20 of IC15, pin 12 (FOK) of IC16 is at −12 V and Q2 turns OFF. Signal FE through focus gain adjustment potentiometer VR1 is amplified in IC1 (1/2) and input to IC2 (1/2) via the phase correction CR circuit. Then, the signal power-amplified in IC2 (1/2) drives the pickup actuator coil to form a servo loop including the optical pickup by which the laser beam is always focused exactly on the disc pit surface irrespective of the amount of disc warp, etc.

During light emission of the laser diode, the gate of FET Q4 connected to the LDC line is "L" so that IC2 (1/2) performs normal amplification. In addition, the gate of Q6 connected to the FOK line is at −12 V when RF signal is provided. Therefore, Q6 turns OFF and amplification is possible in the loop connecting IC1 and IC2, where the focus servo works.

1-2-2 Tracking servo circuit

Signals S1 (A + B) and S2 (C + D), produced by the preamplifier on the mechanism PCB, are fed into pins 6 and 7 of connector CN6. These signals are partially amplified by a 3-stage amplifier of inverter IC5 to generate the tracking error signal, then waveform-shaped by IC7 and input to TS1 and TS2 of IC15.

The tracking error signal is generated in IC15 and output from TEOP and TEON. This signal works as the tracking servo signal.

On the other hand, signals S1 and S2 are combined via R100 and R101 to extract music signal. The combined signal is input to IC6 which acts as an amplifier like IC5. After 1st stage-amplification, it is further 2-stage amplified through the EFM test point via the second-stage amplifier which is bias-controlled by DSV and is input to pin 17 (EFM I) of IC15.

The tracking error signals output from pins 3 and 4 of IC15 (TEOP and TEON) are combined in IC12 (1/2). The combined output (TE) is phase-inverted in IC14 (1/2) and input via tracking gain trimming potentiometer VR2 to pin 6 of IC1 (2/2) in which it is phase-corrected and amplified.

Further, output of IC1 (2/2) is power-amplified in IC2 (2/2), Q10 and Q11. Amplified TE signal drives the pickup actuator coil to form a tracking servo by which the laser beam spot follows exactly the pit sequence on the disc.

1-2-3 DSV circuit (IC8 (1/2) and IC15 DLS 1 and 2)

Pits are made on a disc in such a way that the sum of "H" durations is equal to that of "L" durations i.e. DSV (Digital Sum Value) is zero. Thus, this circuit controls the amplifier bias so that the data on the disc is identical to that read by the player, thereby decreasing error.

1-2-4 Envelope detection

The signal from pin 4 of IC6 is further amplified and applied to the base of Q21. The variation in amplitude of the DC component, that is equivalent to the amplitude of the EFM signal wave, appears in the emitter of Q21. This DC component is amplified only in low frequency by IC8 (1/2) and applied to the gate of AGC FET Q33, thus reducing the change in EFM signal. In addition, the EFM signal is level-compared in IC10 (1/2). Then "L" at pin 1 of IC10 (1/2) informs to pins 20 (RFOK) of IC15 on SERVO (×29) PCB and 29 (RFOK) of IC15 on the process (X32) PCB through pin 1 of CN7 that the EFM signal is provided.

In addition, the EFM signal is also applied to IC10 (2/2) via diode D19 for level-comparing. Then, it is output from pin 8 as signal RFES. This signal is used in dropout control on play or used in the kick processing circuit at kick of motor.

1-2-5 Pickup carry motor driver

As play advances tracing the disc pit sequence by the pickup, a positive offset voltage appears at the output of tracking coil driver pin 8 of IC2 (2/2) by the tracking servo function. Since the high-frequency component, which is also contained in the tracking driver output besides the offset voltage, is unnecessary for driving the pickup carry motor, it is eliminated by an LPF amplifier of IC3 (2/2). Further, this output is power-amplified in IC4 (2/2) to drive the pickup carry motor.

In addition, Q14 is ON to avoid application of the tracking servo output signal during modes other than play. Signal PUFB, which is entered to the input of the power amplifier (pin 3 of IC4 (2/2)), is used in kick operation or fast movement of the pickup.

1-2-6 Disc motor driver

When pin 15 (MSP) of IC15 on the servo PCB emits an "H" signal according to the CPU command, the gate of Q17 becomes "L" and Q17 turns OFF. Disc motor driver IC4 (1/2) can amplify signal AFC emitted from IC8 on the process PCB due to start the disc motor. Due to shorten the start time or the stop time, a circuit consisting of Q19, C36, Q18 and R94 applies positive or negative pulse to the pin 7 of IC4 (1/2). (Positive pulse at motor's start Negative pulse at motor's stop).

1. CIRCUIT DESCRIPTION

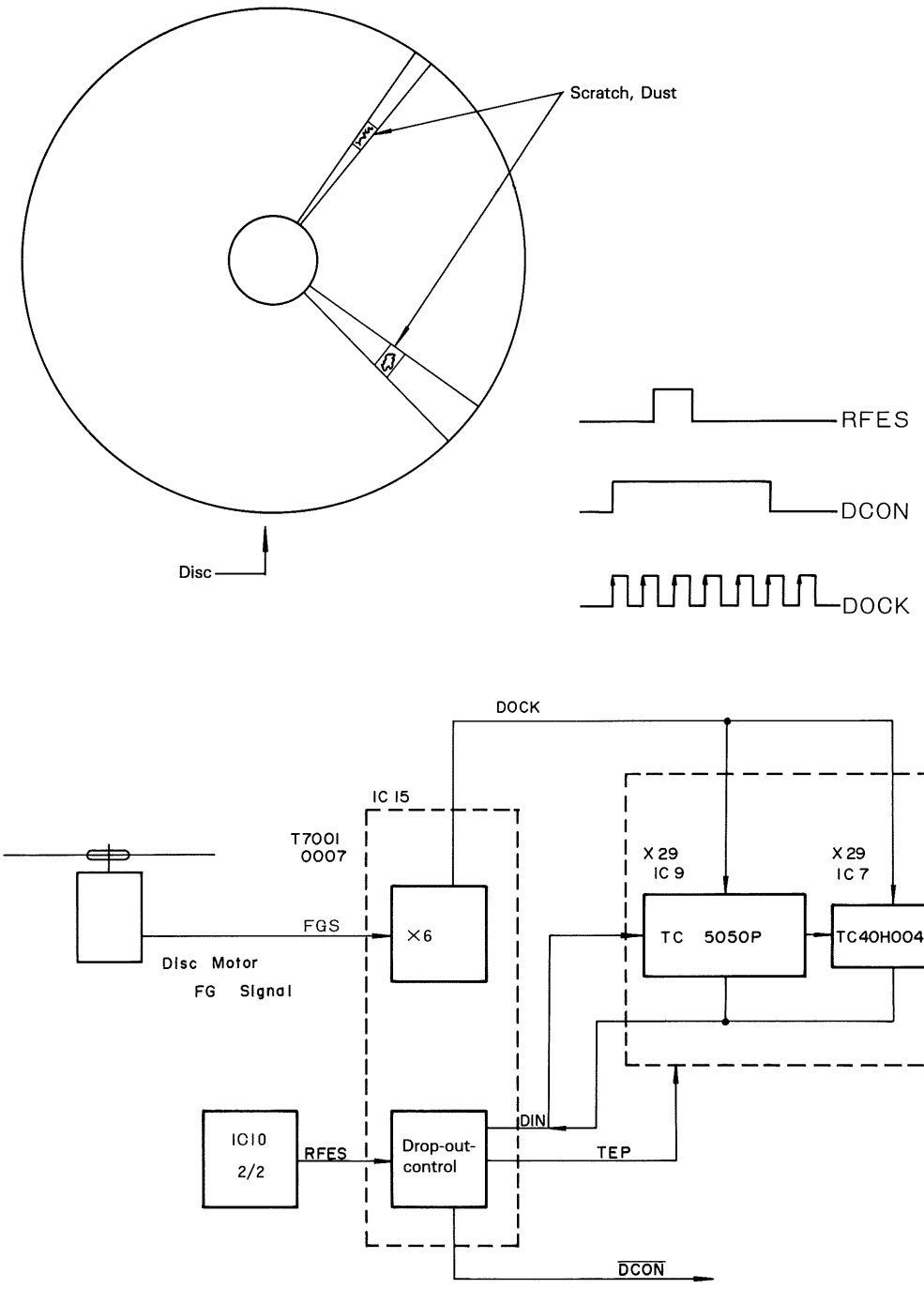


Fig. 1-2A

1. CIRCUIT DESCRIPTION

1-2-7 Tray motor driver

3-state output situation in pin 9 of IC15 is used for driving the tray motor. The signal at "H" is inversion-amplified in IC3 (1/2) to drive Q16 to make pin 3 of CN4 negative so that the tray motor rotates in the direction in which the tray is closed. Conversely, the signal at "L" is also inversion-amplified in IC3 (1/2) to turn ON Q15 so that the tray motor rotates in the direction in which the tray is opened.
In addition, when pin 9 of IC15 is opened, pin 2 of IC3 is at zero voltage so that the tray motor stops since no voltage is applied.

1-2-8 Tracking error detector control

(This circuit is effective only at kick operation.)
Both IC12 (2/2) and IC13 (1/2) output "H" signals in normal operation. Thereupon, when the tracking error voltage at pin TE output goes up more than about +0.6 V, pin 2 of IC12 (2/2) becomes "L" and this voltage is applied to TEG 1 input of IC15. See "1" in the table below.

State	TE Voltage	TEG1	TEG2
1	> +0.6	L	H
2	< −0.6	H	L

Table-1

Conversely, when the tracking error voltage at TE output goes down less than −0.6 V, pin 2 of IC12 (2/2) becomes "H" and pin 2 of IC13 (1/2) "L" so that this voltage is applied to TEG 2 input of IC15. See "2" in the table above. The search time is shortened by this control circuit. Normally, in play mode, this voltage is offset by signal TEP, therefore inputs TEG 1 and TEG 2 are invalid.

1-2-9 Peak hold circuit

The peak hold circuit consists of Q23 to Q26, D28 to D35, IC14 (1/2), etc. When KGC becomes "H" on kick state, Q23 and Q24 turn ON, and Q25 and Q26 turn OFF. Thereby, C70 is charged with the positive peak voltage at tracking error input TE and C69 is charged with the negative peak voltage.
During kick, C69 and C70 are continuously charged with these peak voltages. When the unit returns to normal play from the kick state, Q23 and Q24 turn OFF and Q25 and Q26 turn ON. Then, the average value of the voltages at C70 and C69 is input to IC14 (1/2). Here, it is subject to subtraction with the value of voltage TE, so that the unit is restored to normal play from the kick state.

1-2-10 TE noise limiter

This noise limiter consists of IC14 (2/2) and Q27 to Q30. Q29 is the limiter ON/OFF switch. When signal TEP is "L" (during kick), no limiter operation is possible. Normally, Q29 is OFF during play.
The tracking error (TE) voltage is amplified to about 6 times in IC14 (2/2) and is applied to the bases of Q27 and Q28 through an HPF consisting of C73 and others. When the voltage goes up more than about +0.6 V, Q27 turns ON, while when it goes down less than about −0.6 V, Q28 turns ON. During that ON period, the peak noise of the voltage is suppressed so that the following stage gets free from the disturbance caused by this noise. Thereby, the pickup is prevented from jumping off the correct track to another one due to noise.

1-2-11 Disc flaw position memory circuit (See Fig. 1-2A.)

Signal RFES produced in IC10 (2/2) becomes "H" when the RF signal level is discreased by flaws or dust on the disc. This signal at "L" is output as signal DIN from the dropout control block in IC15 to the disc flaw position memory circuit in which positional data of flaw is stored. At the same time, this signal is also output as signal DCON which is the tracking servo gain reduction gate pulse. Dropout control is thus made.
Pin DIN of IC15 outputs a signal indicating the RFES state at the rising edge of signal DOCK. It also checks the output of the disc flaw position memory circuit (pin 8 of IC7) at the falling edge of signal DOCK and then outputs signal DCON (pin 12 of IC15) to tracking servo amp circuit.

1-2-12 Relationship between servo and control line

For play, the actuator of the pickup is moved up or down by the 2 Hz signal from F.SRCH (pin 2 of CN2). At this time, when the disc is in rotation, the RF signal is output from the pickup only at the moment the laser beam is focused. With the RF signal, IC10 (1/2) outputs an "L" signal (RFOK) to turn ON Q31. Further, this signal is inverted at IC16 and FOK becomes −12 V. Q2 and Q6 is turned off by "L" FOK signal, "H" LDC signal is inverted to "L" to turn Q4 off, so that the focus servo starts operation. Thus, a continuous RF signal appears at pins 6 and 7 of CN6 from the pickup. Thereby, pin 14 (FOKG) of IC15 outputs an "H" signal. This signal is inverted at IC16. The voltage at pin 11 of IC15 becomes −12 V. Therefore, Q12 turns OFF so that IC2 (2/2) can perform amplification. In addition, DCON is "L" as long as the level of the RF signal does not drop suddenly due to flaws or dirt on the disc. As the KGC line is at −12 V in normal play (except for the kick state), Q7, Q8, Q9 and Q12 are all OFF. Thus, the tracking servo works so that the pickup traces the pit sequence on the disc. The data on the disc can thereby be read out continuously.

1. CIRCUIT DESCRIPTION

1-3 PROCESS CIRCUIT

1-3-1 EFM signal demodulation

The EFM signal (EFMO) output from pin 41 of IC15 on the servo PCB is input to pin 52 (EFM 2) of IC8 and pin 14 (EFMI) of IC9 on the process PCB.

IC9 works as a digital PLL together with VCO Q3. Signal EFMI is phase-compared with signal PLCK (4.32 MHz) resultant from 1/4 frequency division of signal VCOI.

Here, when signal PLCK is delayed from signal EFMI, pin U_{OUT} becomes "L" and acts to make the VCO frequency higher. Conversely, when it is advanced, pin D_{OUT} becomes "H" and acts to make the VCO frequency lower.

The EFM signal output from pin D_{OUT} in synchronization with the rising edge of signal PLCK is fed to pin 53 (EFMI) of IC8, in which detection is made to a frame sync signal which is a continuous signal of 11 "H" bits and 11 "L" bits.

When the frame sync signal is obtained, the EFM signal is demodulated into an 8-bit signal. Moreover, the user's bits just after the frame sync signal are demodulated and data Q among them are displayed as time data bundled by 98 frames. These are also used in FF or BWD operation, etc.

The music data, converted from 14-bit to 8-bit signals, are written in jitter absorption memory IC7 under control of IC6 (TC9179F). The one-frame 32-symbol data is corrected for error in the C1 correction section. Next, after de-interleave operation, the data which could not be corrected in the C1 correction section is corrected in the C2 correction section.

Only the data which could not be corrected even in the C2 correction section is subject to mean-value interpolation and is output to the D/A converter.

1-3-2 CLV servo control in IC8 (TC9178F)

a) AFC

The signal resultant from 1/4 frequency division of frame sync signal and the input signal (2.1168 MHz) from C21K are used here. Then, with the center of the count of 1152 clock pulses of C21K in respect to the former signal, pin 20 (AFCO) outputs a 0 V signal when the speed of the disc motor rises about 10% and outputs a 5 V signal with the same voltage as voltage VDD when the speed lowers about 10%. Thus, in the range of ±10% change in motor speed, the output voltage corresponds to motor revolution (PWM wave).

b) APC

Phase-comparison is made between the signal resultant from 1/8 frequency division of the frame sync signal and the signal from a frequency division of signal C21K. The comparison output is emitted as PWM signal with 8-bit resolution. Here, VDD/2 (2.5 V) is output at a phase difference of zero in a control range of $\pm 7/8\ \pi$.

In addition, the speed of the disc motor can be controlled by signal DIV+ or DIV- from TC9179F. For information about TC9178F and TC9179F, refer to the diagram on pages 81 to 90.

1. CIRCUIT DESCRIPTION

1-4 D/A converter

The serial music data, which is output from IC6 on the process PCB, is input to the D/A converter (IC21) at the falling edge of signal BCK. The data of one word is transferred to IC21 by repeat input at 16 cycles of signal BCK. After that, when signal CC drops down to "L", a pulse (DCR or DCL) is output with which the integrator output is discharged. Then, after clearing the previous sampled value, signal IOUTR or IOUTL is continuously output according to the level of signal LRCK during the time in proportion to the amount of the digital music data and is held as an analog voltage at integration capacitor C212 or C213. The example of waveform ① in Fig. 1-4A represents a sequence of this state. ② Fig. 1-4A shows the waveform when signal IOUTR or IOUTL is sampled by signal LRCK. When this PAM wave is filtered by an LPF, this LPF outputs a music signal with a peak amplitude of 1/2 that of the PAM wave. This music signal is input to buffer amplifier IC27 to which a frequency characteristic compensotor CR circuit is connected.

IC26 controls the emphasized signal detected by IC8. Pin EMPH of IC8 outputs an "H" signal with a disc on which emphasized signals are recorded, and thus the de-emphasis circuit works. The muting relay connected to the output pin is controlled by the muting signal from the micro-processor. In addition, IC21 judges the music data as an R-ch signal while signal LRCK is "L". During this period, IC6 outputs L-ch signals. Therefore, signal IOUTR of IC21 is handled as an L-ch signal and signal IOUTL as an R-ch signal.

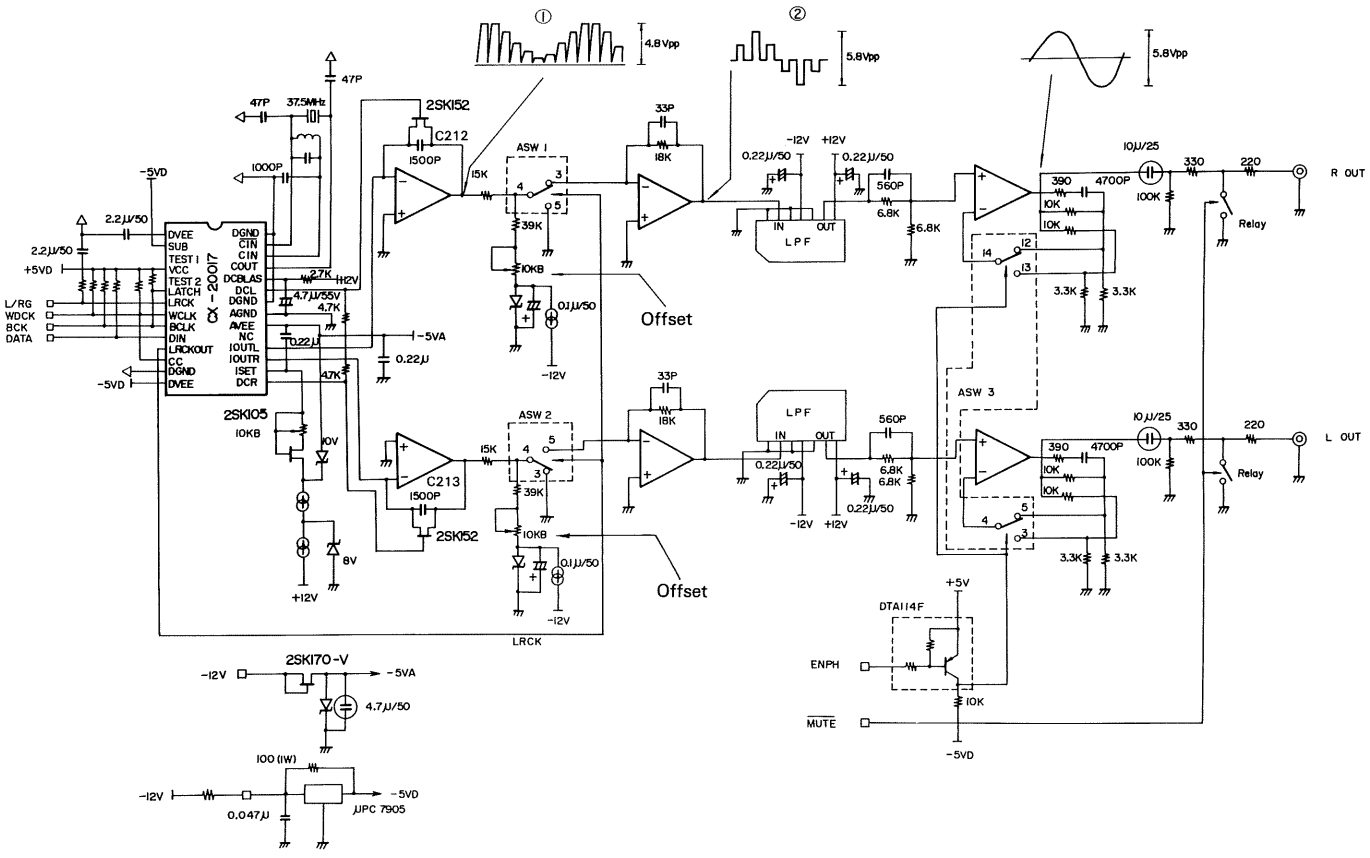


Fig. 1-4A D/A Converter Circuit

1. CIRCUIT DESCRIPTION

1-5 MAIN CIRCUIT OPERATION

1-5-1 RESET OPERATION

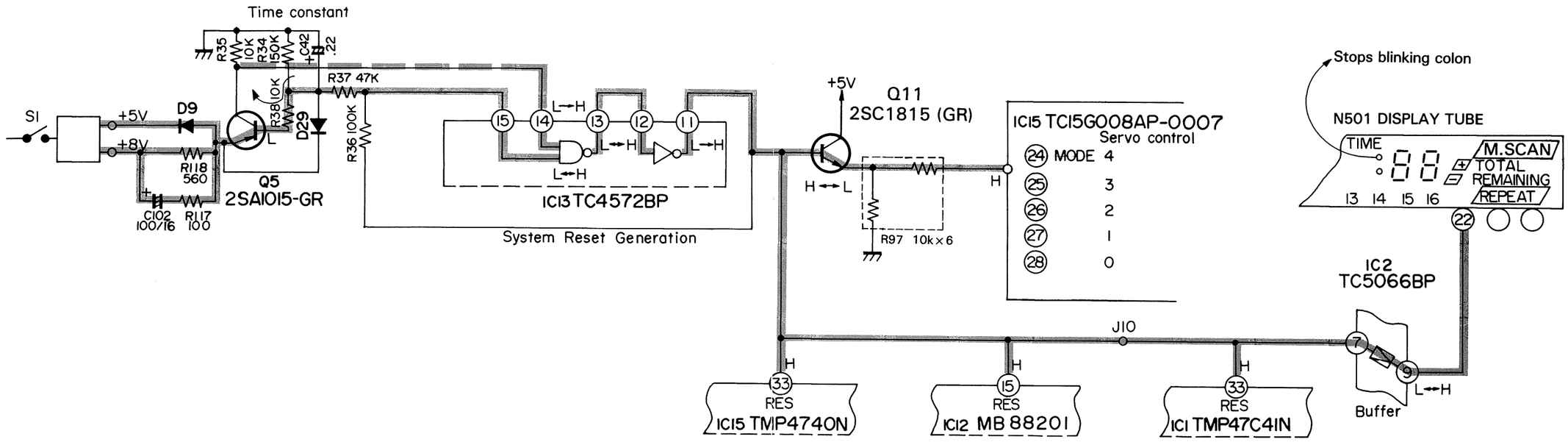
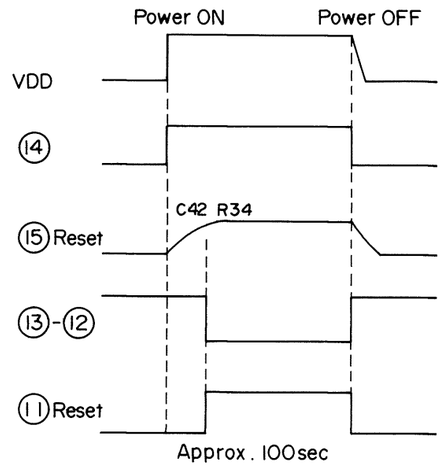


Fig. 1-5-1-1

1. When power switch S1 is turned on, +5 V and +8 V are supplied to the RESET circuit from the voltage regulated power supply circuit.
2. The rising time and the falling time of the power supply voltages +5 V and +8 V are different (+8 V rises faster than +5 V when the power is turned on and it falls faster when turned off.) This creates a difference in operation timing to the microprocessor ciruit (+5 V) and the analog circuit (+8 V). Diode D9 clamps +8 V until +5 V rises, so that the timing difference can be eliminated.
3. When +5 V rises, it is supplied to the emitter of Q5. Q5 turns on, producing about 5 V at its collector. It is coupled to pin 14 of IC13 and puts it to "H" level. When the emitter of Q5 is provided with about 5 V, the base voltage becomes about 4.4 V due to time constants R34 and C42. This "H" level signal is applied to pin 15 of IC13.
4. When both of pin 14 and 15 are at "H" level, the level of pin 13 changes from "H" to "L". The inverted output is obtained at pin 11, after going through pin 12. pin 11 is set at "L" level by R36, but it changes the level from "L" to "H". (This signal is termed reset signal.)
5. When the reset signal is "H" level, IC15 (TMP4740N), IC12, IC1 and IC15 (TC15G008AP-0007) start functioning. IC15 (TC15G) is, however, reset via Q11 in order to avoid the overloading at pin 11 of IC13. When Q11 is OFF, modes 0 through 4 are at "L" level by means of R97.
6. When power switch S1 is turned OFF, +8 V drops, making the emitter voltage of Q5 also drop. When +8 V drops by 1 V, the emitter voltage of Q5 goes down to about 4 V, because about 3 V discharge voltage is being provided by C102 connected across R118. Since the base voltage of Q5 is charged by C42, it does not drop very quickly. Q5 is placed under OFF state. The collector voltage drops, making pin 13 of IC13 to "H" level and pin 11 to "L" level. IC15 (TMP4740N), IC12, IC1 and IC15 (TC15G) stop functioning.



*"H" level: more than 3.5 V
"L" Level: less than 1.5 V

Fig. 1-5-1-2 Timing Chart for IC13 Reset Signal

1. CIRCUIT DESCRIPTION

1-5-2 TRAY OPERATION

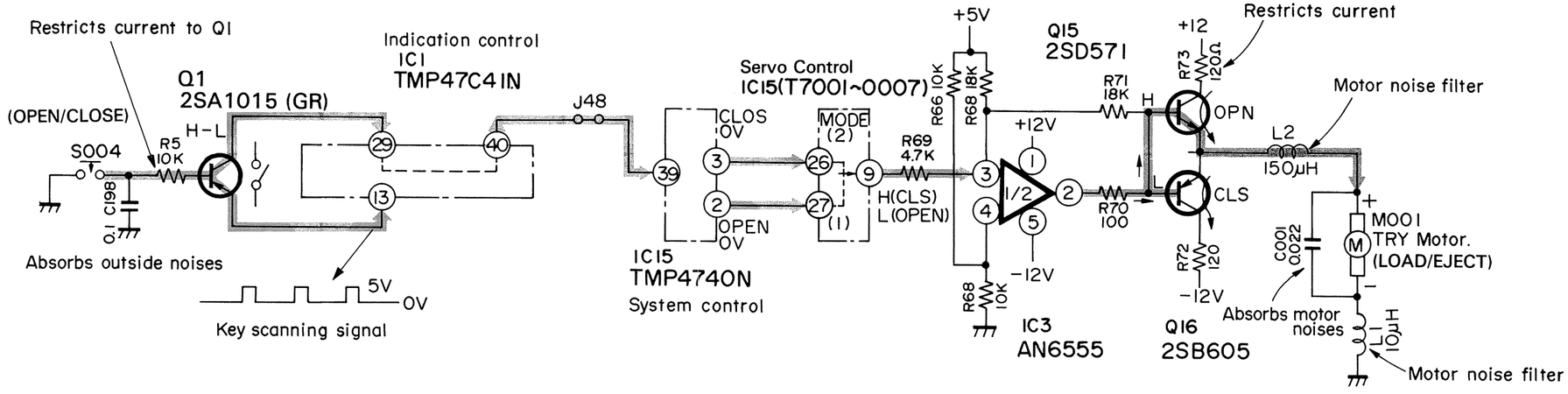


Fig. 1-5-3

1. When tray OPEN/CLOSE switch S004 is pressed, Q1 momentarily turns on and a key scanning signal available from pin 13 of IC1 is applied to pin 29 of IC1.
2. The signal put through pin 29 is processed in IC1 and its output is coupled to pin 39 of IC15 (TMP4740N) through pin 40.
3. The data signal fed through pin 39 controls pin 1 to 5 in IC15. (An instruction signal to IC15 (TC15G or T7001) is developed by a combination of pin 1 to 5.)

TRAY / Control Mode / Pin	OPENS		CLOSES		Remarks
	E	F	8	C	Refer to control MODE of IC15 (TC15G008AP) Table 2-2B and notes below.
1	L	H	L	L	
2	H	H	L	L	
3	H	H	L	H	
4	H	H	H	H	
5	L	L	L	L	

***Notes on Control Mode in Tray OPEN/CLOSE operation**

E: The SLT (start limit) switch is ON, i.e. the tray is retracted and the pickup is moved toward the center of the disc till pickup start limit switch is on. This occurs when the tray is retracted with or without disc by OPEN/CLOSE switch.

F: The SLT switch is OFF. This occurs in the state other than mentioned above such as in PLAY mode or PAUSE mode during playback.

8: The laser diode is ON. This occurs when the tray is closed by pressing PLAY button or any kind of music selection or playback button.

C: The laser diode is OFF. This occurs when the tray is closed by pressing OPEN/CLOSE switch.

4. When the power is turned on and tray OPEN/CLOSE switch is pressed, the tray opens. When the switch is pressed again, it closes. The operation is repeated alternately by every pressure of OPEN/CLOSE switch (S004)
5. The OPEN/CLOSE function of the tray is achieved by combinations of ''H'' and ''L'' levels at pin 1 to 5 of IC15 (TMP4740N) as shown below.
6. The outputs from pin 1 to 5 of IC15 (TMP4740N) are applied to pin 24 to 27 and 30, and the output is then available at pin 9 of IC15 (TC15G or T7001).
7. Pin 9 of IC15 (TC15G of T7001) has a high impedance for the conditions other than the listed left. The input to pin 3 of IC3 is +2.5 V, which is obtained by dividing +5 V with R68 and R71. The +5 V is also divided by R66 and R67 to provide pin 4 of IC3 with +2.5 V. The comparative difference between voltages at pin 3 and 4 of IC3 is available at pin 2 as an output. Since the voltages at pin 3 and 4 are the same +2.5 V, the resultant output at pin 2 becomes 0 V. When the voltage at pin 2 of IC3 is 0 V, Q15 and Q16 are OFF and the tray motor does not run with no power supplied.
8. When the tray opens, pin 9 of IC15 (TC15G or T7001) is at ''L'' level. It pulls down the potential at pin 3 of IC3 from 2.5 V down toward ground. The inverted output changing (from 0 V) toward plus appears at pin 2. It turns on Q15. The motor revolves in the clockwise direction. (Q15 and Q16 prevent overloading of pin 2 of IC3.)
9. When the tray closes, pin 9 of IC15 (TC15G of T7001) is at ''H'' level. It pushes the voltage at pin 3 of IC3 from 2.5 V up toward power supply voltage. When the voltage at pin 3 becomes higher than that of pin 4 (2.5 V), the inverted output changing (from 0 V) toward minus appears at pin 2. It turns on Q16 (while Q15 is OFF), providing the tray motor with a minus voltage, which comes from −12 V line through R72 and L2. The motor revolves in the counterclockwise direction.
10. When the OPEN/CLOSE function of the tray is completed by pressing the tray OPEN/CLOSE Switch, a leaf switch provided on the tray turns ON or OFF. The state of the switch is given to IC15 (TMP4740N) to control the signals at pin 1 to 5 and the motor stops revolving.

1. CIRCUIT DESCRIPTION

1-5-3 LASER ON OPERATION

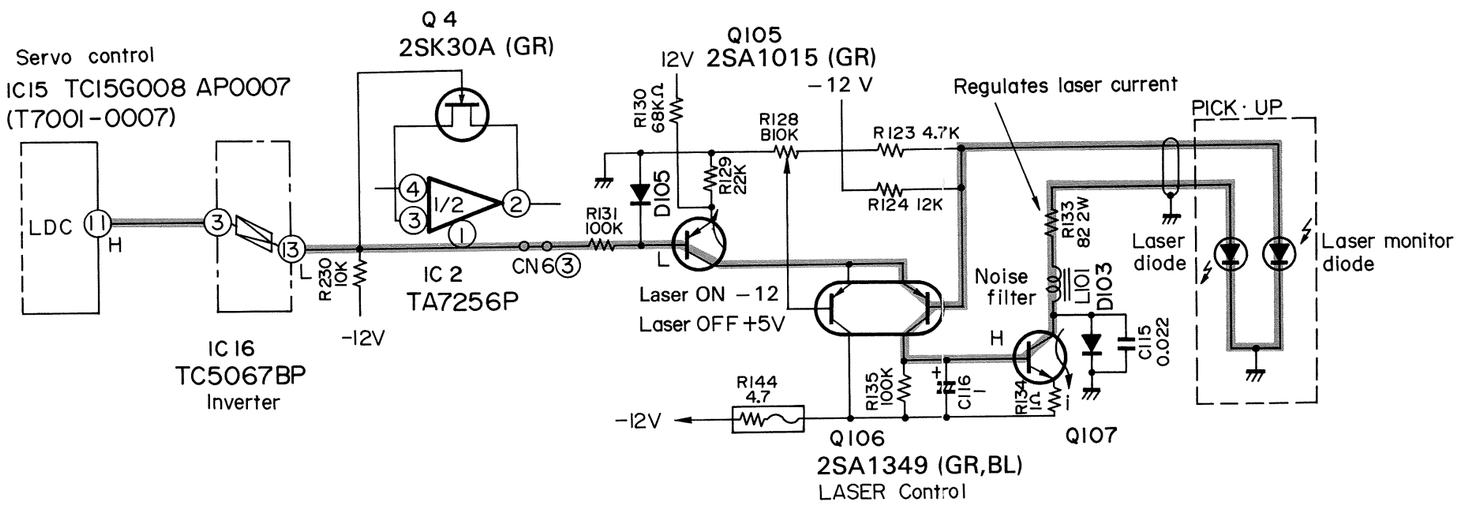


Fig. 1-5-3-1

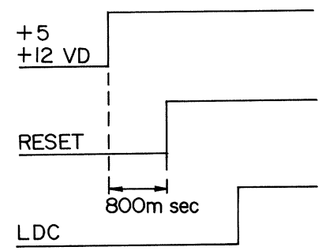


Fig. 1-5-3-2 Timing diagram for LASER ON TIME.

1. When a signal to activate the laser is applied to pin 24 to 27 of IC15 (TC15G or T7001) from the system control microprocessor, the level at pin 11 changes from ''L'' to ''H'' and the level at pin 3 of IC16 also switches from ''L'' to ''H''.
2. IC16 output becomes +5 V (power supply voltage of IC16: V_{DD}) at pin 13, when input pin 3 is at ''L'' level. When the input is ''H'' level, the output becomes open. The output at pin 13, however, becomes −12 V, since it is connected with a −12 V line through R230.
3. When the voltage at pin 13 of IC16 changes from +5 V to −12 V, Q105 turns ON. (+12 V is divided by R129 and R130 to provide the emitter of Q105 with about 3 V. When the base voltage drops below 3 V+0.6 V, it makes Q105 turn ON.) Q106 also turns ON.
4. When Q106 turns ON, a voltage is developed across R135 connected to the collector. Q107 switches ON and it draws a current through the laser diode to emit laser beam. When the diode emits laser beam, a monitor diode provided in the pickup assembly watches the laser emission. The emission can be held constant by controlling the current through Q107 with a help of the monitor diode.
5. Q106 consists of two transistors with the identical characteristics, being used under the same conditions (same emitter voltage and current). Therefore, it functions to produce the same base voltage. When laser current control R128 is adjusted, the base voltage of the other transistor is also affected (the voltage is determined by R123, R124 and the laser monitor diode.)
   The values of R123 and R124 are properly selected depending on the pickup used.
6. When a voltage is increased across R135 placed in the collector of Q106, it provides the base of Q107 with a voltage in accordance with this collector voltage. The collector current of Q107 changes accordingly, thereby controlling the output of the laser diode.
7. When the output of the laser diode increases, the internal resistance of the laser monitor diode becomes small. The base voltage of Q106 gets higher, thereby reducing the current through Q106. The voltage across R135 in the collector circuit drops and it provides the base of Q107 with a lower voltage. Its collector current is reduced to produce less output from the laser diode.

1. CIRCUIT DESCRIPTION

1-5-4 FOCUS SEARCH OPERATION

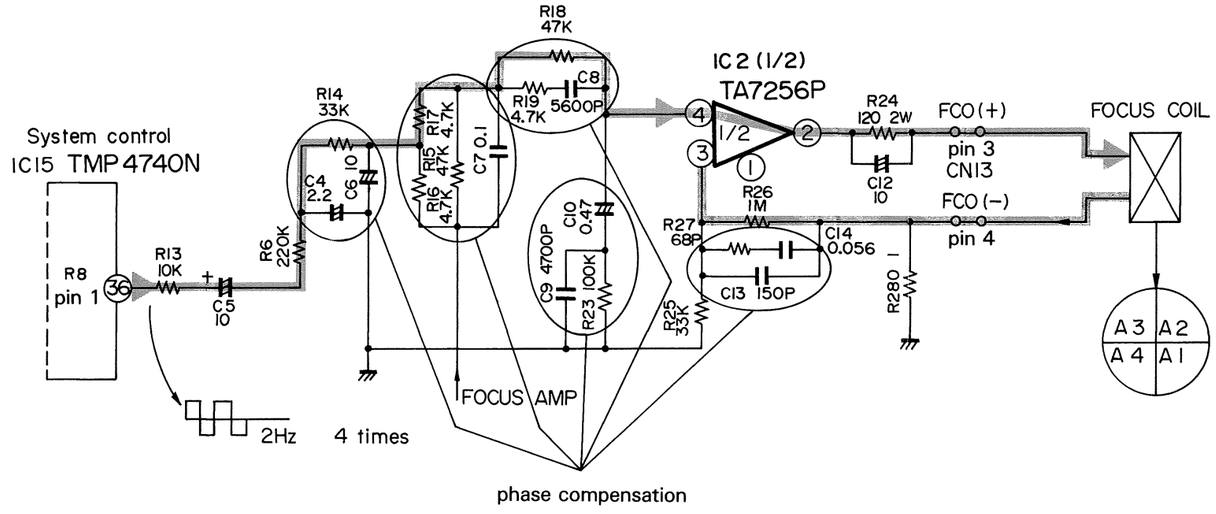
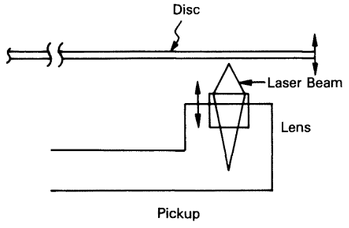


Fig. 1-5-4-1

1. When a disc is set and the tray is closed , a signal of 2 Hz is output maximum four times to pin 36 of microprocessor IC15 (TMP4740N). This signal confirms that the disc has been properly set and prepares for focus servo operation.
2. The focus servo maintains a constant position of the pick-up lens against the disc so that the size of the focused laser spot is kept constant as a result. If the distance between the pickup and the disc is too far or too close, a proper size of the laser spot can not be obtained on the disc surface, in another words, not properly focused.



3. A proper size of the laser spot is provided on the disc surface by moving the pickup lens up and down using the 2 Hz signal. This is called focus search operation. Once it is focused, the search signal is discontinued.
4. The output signal from pin 36 of microprocessor IC15 is applied to pin 4 of focus coil drive amp IC2 (1/2) via R14, R17 and R18. (The focus coil moves the pickup lens up and down.) Its output appears at pin 2 and is applied across the focus coil to move the lens up and down.
5. C5 in the above schematic diagram cuts off the DC component of the signal and R6, C4, R14 and C6 form a LPF to eliminate frequency components higher than 2 Hz.
6. The phase compensation circuit (compensates the frequency characteristic and phase charateristic of the pickup) in the above diagram is for the focus servo purpose. Refer to focus servo operation (1-5-7).

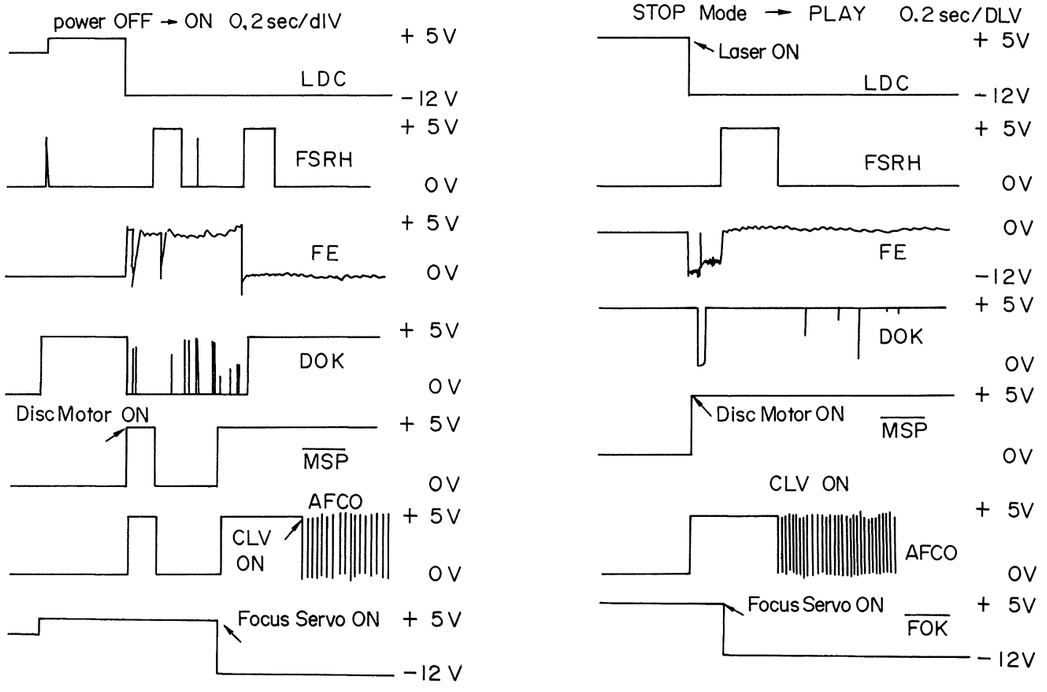


Fig. 1-5-4-2 Operation Timing of Focus Search

1. CIRCUIT DESCRIPTION

1-5-5 DISC DETECTION OPERATION & REVERSE-REVOLUTION PREVENTION CIRCUIT FOR DISC MOTOR

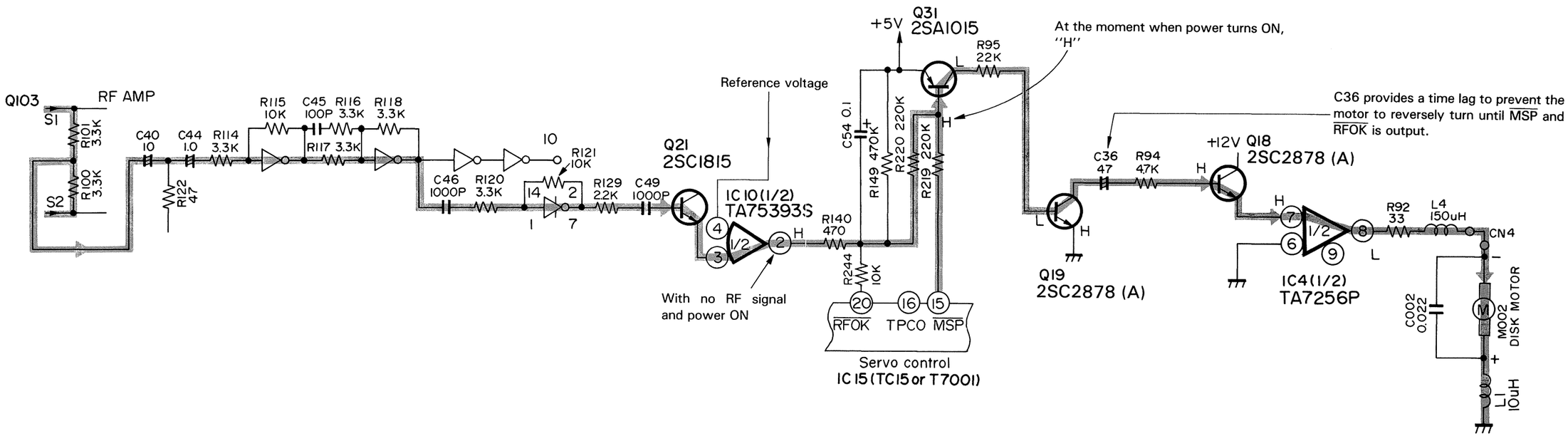


Fig. 1-5-5

1. An RF signal is produced by adding output signals S_1 ($A_1 + A_3$) and S_2 ($A_2 + A_4$) from the 4-devision photodetector through R101 and R100 and amplified to an adequate level. It is then envelope detected by Q21. The detected signal is applied to pin 3 of IC10 (1/2). On the other hand, a signal of reference level (about 0.8 V), which is divided by resistors, is fed to pin 4 of IC10 (1/2). The detected signal and reference level is compared and output to pin 2. That is, when the envelope of RF signal is over 0.8 V, "L" (about 0 V) output results and when it is less than 0.8 V, "H" (about 5 V) results.
2. The time constant for transition to "H" signal or to "L" signal is different. The time constant for transition to "H" is determined by C54 and R149, and the time constant for it to "L" is determined by C54 and R140. The time constant for "H" is about 1000 times larger than that for "L". This prevents the output from accidentally becoming "H" because of dropouts of RF signals caused by scratches or dusts. It also falls to "L" quickly, when RF signal ($\overline{\text{RFOK}}$ Signal) is detected.
3. The RFOK signal is to judge the presense of RF signal as explained above. It results in "L" when the RF signal is present and it results in "H" when not present. Both of the $\overline{\text{MSP}}$ and $\overline{\text{RFOK}}$ signals are "H", when the disc motor starts running (initial start from a complete stop state.) Q31 and Q19 go to OFF, while Q18 is ON. This increases a negative voltage at pin 8 of IC4 (1/2), thereby preventing the disc motor from revolving in the reverse direction.

1. CIRCUIT DESCRIPTION

1-5-6 FG & DISC MOTOR DRIVE AND STOP OPERATIONS

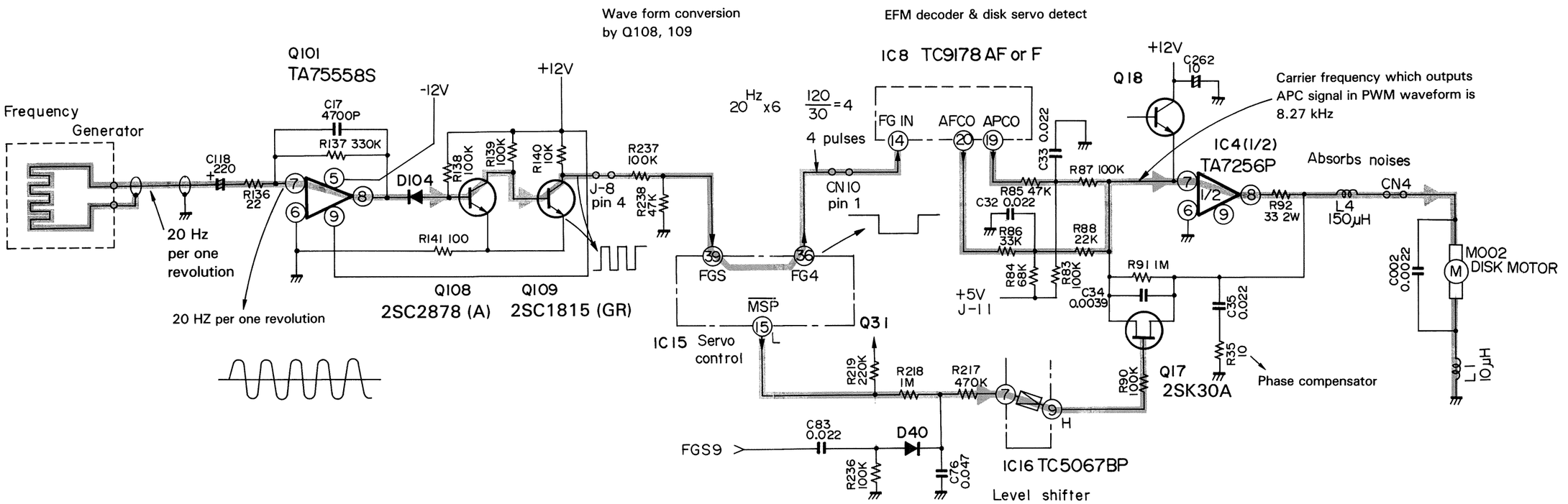


Fig. 1-5-6

1. The frequency generator consists of a polarized magnetic ring attached to the rotating spindle of the disc motor and a printed pattern in the form of coil, which is provided at a relative position below the motor spindle. When the motor revolves, a 20 Hz pulsive current with is sent out per each revolution of the motor.
2. It is fed to pin 7 of Q101 and a sine wave signal with an amplitude of ±5 V is available at pin 8. It is converted into a pulse signal by Q108 and Q109, divided to a TTL level by R237 and R238 and then applied to pin 39 of IC15 (TC15G or T7001) as FGS. The FGS is 6 times multiplied in IC15 (TC15G or T7001) to be DOCK output and 1/30 divided to give FG4 at pin 36. Since the FGS includes 20 pulses per one disc motor revolution, the DOCK contains 120 pulses per a revolution and the FG4 includes 4 pulses.
   The DOCK is used to detect a dropout position (Refer to section 1-5-15). The FG4 is coupled to pin 14 of IC8 (TC9178F) of detect the revolution of the disc motor.
3. The revolution control of the disc motor is accomplished by APCO (from pin 19) and AFCO (from pin 20). Both of the signals are PWM (pulse-width modulation) signals with a carrier frequency of 8.27 kHz in the CLV mode. When a disc is revolving at a normal speed, both of the AFCO and APCO are clock waveform signals with a frequency of 8.27 kHz at a 50% duty. Since the AFCO regulates a range of zero revolution to high revolution of the disc motor, it may be fixed at ''H'' or ''L'' level in some instances.
4. The APCO and the AFCO are integrated by R85 and C33, and R86 and C32 respectively. They are then added via R87 and R88. The added signal is put to pin 7 of IC4 (1/2). The output signal goes through a low-pass filter to regulate the disc motor revolution. C35 and R35 are for phase compensation. L204 is a noise filter.
5. Q17 is in an OFF state during normal play. It is ON when the disc motor is not running, providing 0 V output from IC4 (1/2). This ON/OFF operation is achieved by $\overline{\text{MSP}}$ and FGS. $\overline{\text{MSP}}$ is an output signal made available at pin 15 of IC15 (TC15G of T7001) by the microprocessor. When it is at ''H'' level, Q17 is turned OFF and the disc motor is driven to run.
6. Since the FGS provides 20 pulses per one revolution of the disc motor as explained previously, it makes pin 7 of IC16 ''H'' level through D40 during the revolution of the motor and Q17 is turned OFF. If disc stops revolution and the FGS becomes ''L'', Q17 turns ON to stop the disc motor. Thus an accidental rotation of the disc by noises or disturbances is prevented.

1. CIRCUIT DESCRIPTION

1-5-7 FOCUS SERVO OPERATION

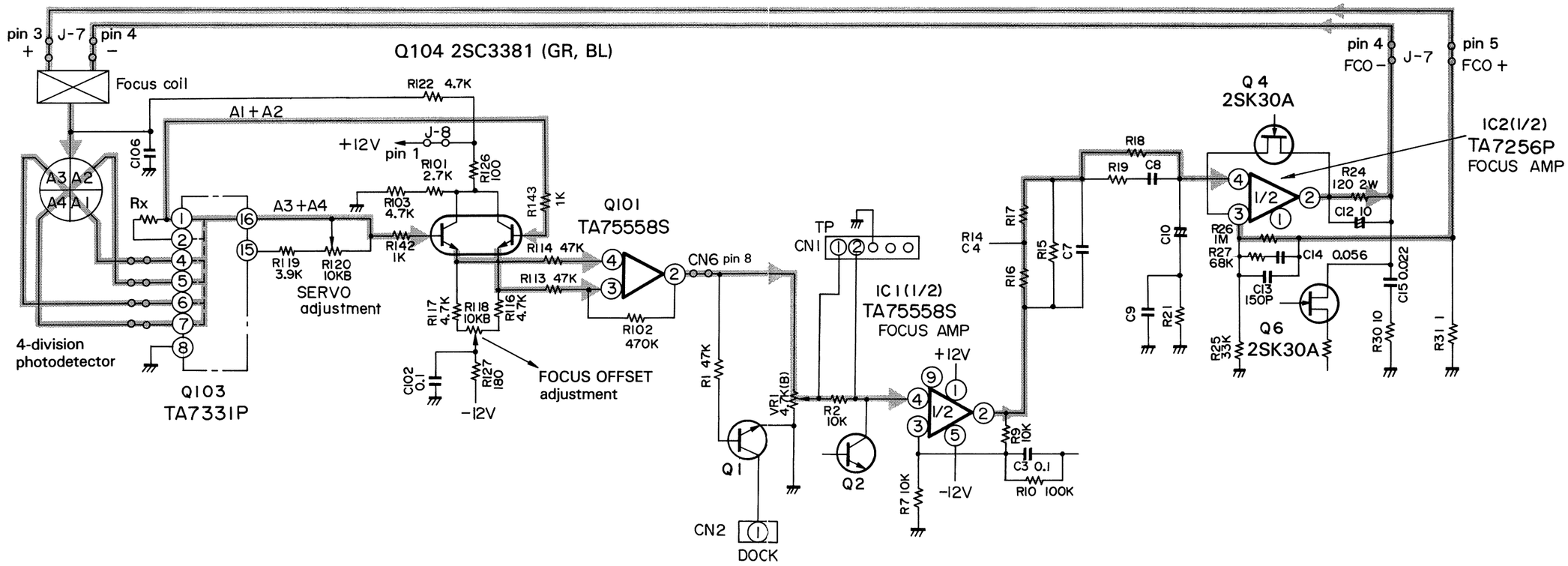


Fig. 1-5-7

1. When laser is ON and a focus search signal is given by microprocessor IC15 (TMP4740N), the reflecting beam from the surface of a disc is detected by a 4 division photodetector and these signals are sent to pin 4 to 7 of head amp Q103 as a variation of current. Inside Q103, A_1 and A_2 are added and output from pin 1, A_3 and A_4 are added and output from pin 16 respectively. The output level from pin 1 of Q103 is varied by Rx, which is in turn changed by controlling SVC switch IC (Q102) from SVC control microprocessor IC12. The output level at pin 16 of Q103 is variable by R119 and focus error balance R120.
2. The outputs from pin 1 and 16 of Q103 are input to each base of Q104 and the focus signal offset is adjusted by R118. The outputs from emitters of Q104 is input to Q101 to obtain the difference of S_1 and S_2 as focus error (FE) signal at pin 2 of Q101.
3. The FE signal is applied to pin 4 of IC1 (1/2), through focus gain adjustment trimming potentiometer VR1 and R2 for monitoring gain adjustment.
4. Q1 turns ON to inform microprocessor IC15 (TMP4740N) that a disc has been properly set, when the 4-division photodetector detects a reflecting beam from the disc.
5. When a reflecting beam from the disc is received, pin 2 of comparator IC10 (1/2) switches its level from "H" to "L". Q31 turns from OFF to ON, changing the collector of Q31 from −12 V to +5 V. The change is input to pin 4 of inverter (IC16). The output of the inverter (pin 12) changes from +5 to −12 V and turns Q2 and Q6 OFF. Thus, a focus loop is formed. Q4 is ON to reduce the gain of the focus amplifier until laser beam is emitted, but it turns OFF after laser has been emitted.
6. The output from pin 2 of focus amp IC1 (1/2) is applied to pin 4 of focus amp IC2 (1/2) through a phase compensation circuit. The output is available at pin 2 and the lens attached to the focus coil is moved up or down in accordance with the output.
   The phase compensation circuit works to secure an appropriate movement of the lens in accordance with the FE signal by compensating changes of sensitivity characteristic and phase characteristic of the focus coil and the pickup.

1. CIRCUIT DESCRIPTION

1-5-8 TRACKING SERVO OPERATION

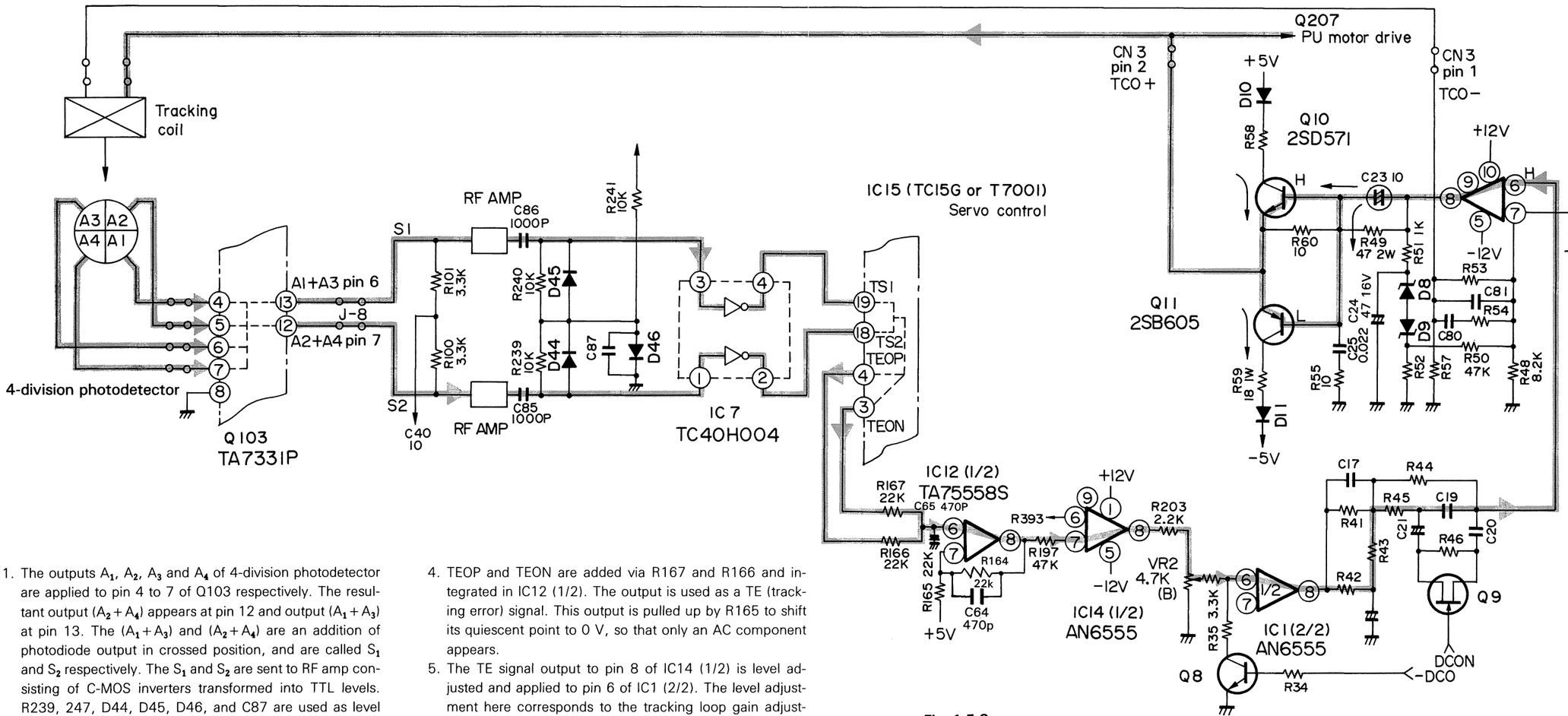


Fig. 1-5-8

1. The outputs A_1, A_2, A_3 and A_4 of 4-division photodetector are applied to pin 4 to 7 of Q103 respectively. The resultant output (A_2+A_4) appears at pin 12 and output (A_1+A_3) at pin 13. The (A_1+A_3) and (A_2+A_4) are an addition of photodiode output in crossed position, and are called S_1 and S_2 respectively. The S_1 and S_2 are sent to RF amp consisting of C-MOS inverters transformed into TTL levels. R239, 247, D44, D45, D46, and C87 are used as level limiter.
2. TS_1 and TS_2 signals (TTL level converted S_1, S_2 signals) are converted to TEOP (pin 4) and TEON (pin 3) by the phase comparison circuit of IC15 (TC5G or T7001). When the phase of TS_1 is leading that of TS_2, TEOP outputs ''H'' level and TEON outputs ''L'' level when the phase of TS_1 is lagging behind that of TS_2.
3. TEOP produces a few fine pulses at the almost ''L'' level under the normal play condition: On the contrary, TEON is almost at ''H'' level, producing similar fine pulses. The distances between these fine pulses shortens, when the tracking servo is off such as in search period.
4. TEOP and TEON are added via R167 and R166 and integrated in IC12 (1/2). The output is used as a TE (tracking error) signal. This output is pulled up by R165 to shift its quiescent point to 0 V, so that only an AC component appears.
5. The TE signal output to pin 8 of IC14 (1/2) is level adjusted and applied to pin 6 of IC1 (2/2). The level adjustment here corresponds to the tracking loop gain adjustment. The output from pin 8 of IC1(2/2) is fed to pin 6 of IC2 (2/2) via a phase compensation circuit, which compensates changes of sensitivity characteristic and frequency response of the tracking coil to insure the appropriate movement of the pickup lens in accordance with a TE signal.
6. Tracking jump may occur because of an excessive amplitude of TE signal caused by scratches or dusts on a disc. RF signals are dropped out for more than a predetermined period for such a cause as this, the DOC signal becomes ''H'' level to make D8, and Q9 turn ON. This reduces the gain of Q8 and changes the degree of the phase compensation in Q9.
7. The output available at pin 8 of IC2(2/2) is applied to a voltage limiter (limit voltage of about ±5 V) consisting of D9 and D8 and sent to the driver stage in a push-pull circuit consisting of Q10 and Q11. The plus voltage is driven by Q10 and the minus voltage by Q11 in order to regulate the tracking coil of the pickup.

1. CIRCUIT DESCRIPTION

1-5-9. TRACKING ERROR GENERATION AND KICK OPERATION

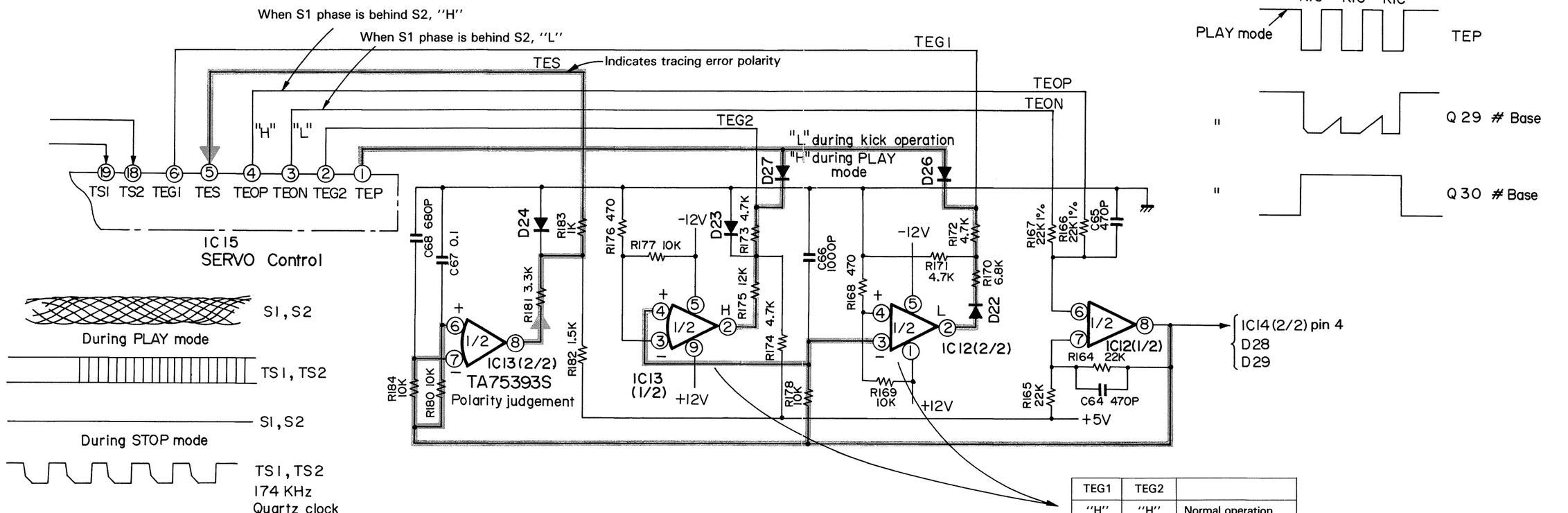


Fig. 1-5-9

TEG1	TEG2	
"H"	"H"	Normal operation
"L"	"H"	TEOP H Output TEON H Fixed
"H"	"L"	TEOP L Fixed TEON H Output

1. Signals (TS1 and TS2), which are available from RF amp IC5 and inverted by IC7, are applied to pin 19 and 18 of IC15 (TC15G or T7001) respectively. TS1 and TS2 are phase compared in IC15 (TC15G or T7001) and the resultant outputs are available at pin 4 (TEOP) and pin 3 (TEON).
2. The TEOP and TEON are added and fed to pin 6 of IC12 (1/2). They are doubled and the output to pin 8. This signal is termed tracking error (TE) signal. The tracking coil for the pickup is moved to offset this signal during normal PLAY mode.
3. During normal PLAY mode, pin 1 (TEP) of IC15 is at "H" level by the mode 0 to 4 signal from microprocessor IC15 (TMP4740N). The "H" signal is applied to pin 6 (TEG1) via D26 and to pin 2 (TEG2) via D27.
4. TEG1 and TEG2 signals are used to control TEOP and TEON signals inside the IC15 (TC15G or T7001), so that the mode can be switched into normal play mode very quickly. The TE signal, output to pin 8 of IC12 (1/2) is applied to pin 4 of IC13 (1/2) and pin 3 of IC12 (2/2) via R178. When the input voltage at pin 4 of IC13 (1/2) is higher than that of pin 3, "H" level is output to pin 2. When it is lower, "L" level is output.
5. Since the input to pin 3 of IC12 (2/2) is an inverted input, when the input voltage of pin 4 is compared, only the difference is inverted and made available as an output at pin 2. The output from pin 2 of IC13 (1/2) is applied to pin 2 of IC15 (TC15G or T7001) and the output from pin 2 of IC12 (2/2) is applied to pin 6 of IC15 (TC15G or T7001), in order to control the circuit for producing TEOP and TEON singals from TS1 and TS2. Since the TEOP is held at "L" level and the TEON at "H" level during a kick operation and the focus-off period, the output from pin 8 of IC12 (1/2) becomes O V and both of the TEG1 and TEG2 are at "L" level.
6. At the end of the kick operation, the output from pin 8 of IC12 (1/2) is applied to pin 7 and 6 of IC13 (2/2). Judging the polarity of the output from IC12 (1/2) (For example, if pin 8 of IC12 (1/2) is minus, the output at pin 8 of IC13 (2/2) is "L" level), the signal is input to pin 5 (TES) of IC15 (TC15G or T7001). The control timing of a kick pulse is determined by this signal in the IC15 (servo control).

1. CIRCUIT DESCRIPTION

1-5-10. SEARCH AND LOCK-IN CIRCUIT OPERATION DURING KICK MODE

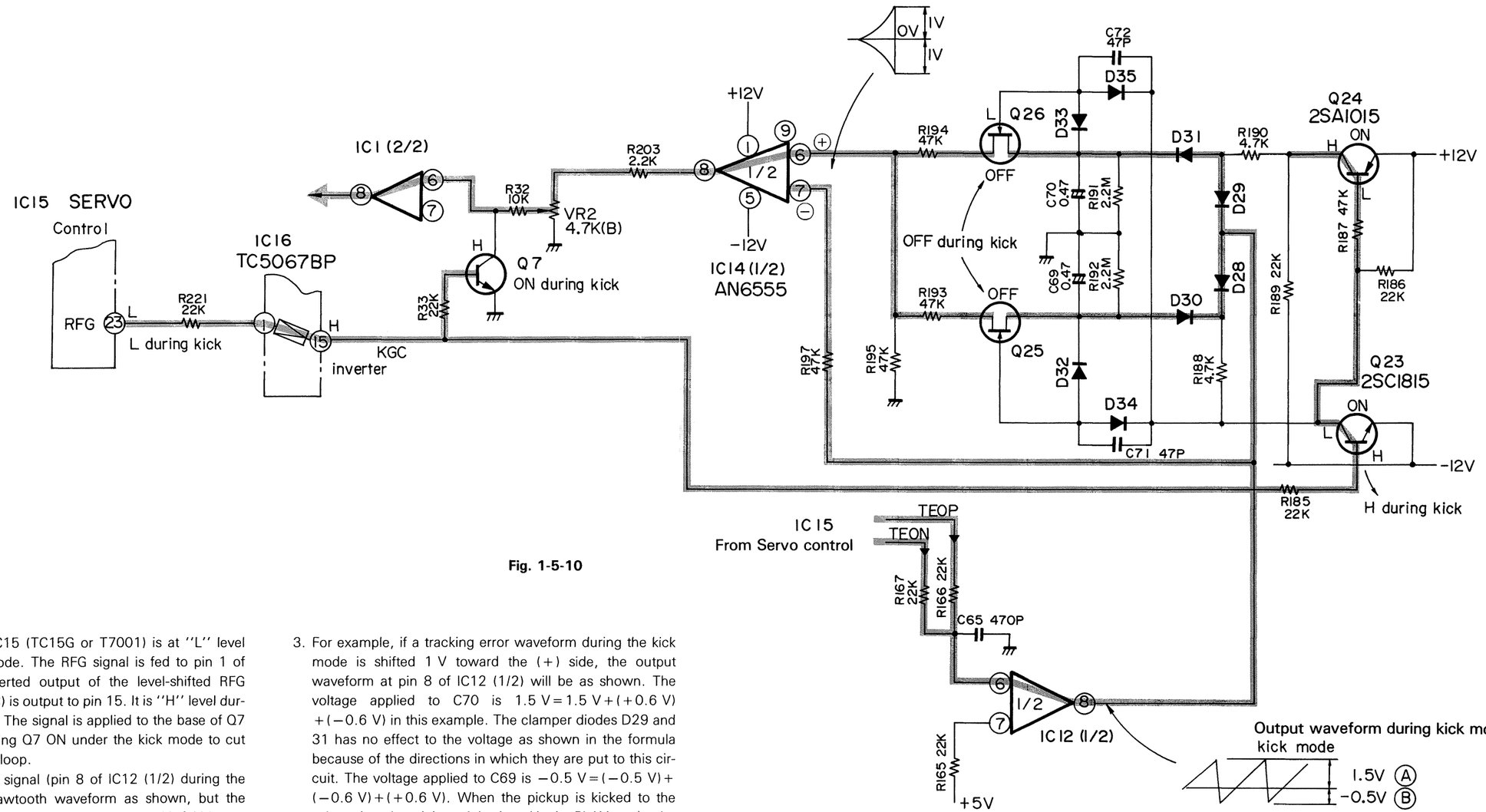
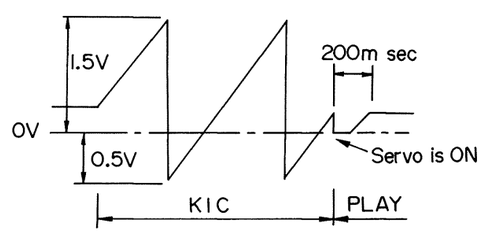


Fig. 1-5-10

1. Pin 23 (RFG) of IC15 (TC15G or T7001) is at "L" level during the kick mode. The RFG signal is fed to pin 1 of IC16 and the inverted output of the level-shifted RFG signal (named KGC) is output to pin 15. It is "H" level during the kick mode. The signal is applied to the base of Q7 through R33, turning Q7 ON under the kick mode to cut the tracking servo loop.
2. The tracking error signal (pin 8 of IC12 (1/2) during the kick mode is a sawtooth waveform as shown, but the center of its amplitude is not always in line with 0 V (some offset results). This may possibly cause unstableness, when the unit changes to a normal PLAY mode from the kick mode (when the tracking servo is ON). To solve this problem, the KGC signal (+5 V during kick mode and −12V during PLAY mode) is given to the base of Q23 through R185, so that Q23 and Q24 are ON, and Q25 and Q26 are OFF during the kick mode.
3. For example, if a tracking error waveform during the kick mode is shifted 1 V toward the (+) side, the output waveform at pin 8 of IC12 (1/2) will be as shown. The voltage applied to C70 is 1.5 V=1.5 V+(+0.6 V) +(−0.6 V) in this example. The clamper diodes D29 and 31 has no effect to the voltage as shown in the formula because of the directions in which they are put to this circuit. The voltage applied to C69 is −0.5 V=(−0.5 V)+ (−0.6 V)+(+0.6 V). When the pickup is kicked to the selected track and the unit is placed in the PLAY mode, the KGC becomes −12 V and Q23 and Q24 turn OFF, making Q25 and Q26 turn ON.
4. The voltages charged across C70 and C69 are added through R194 and R193. In this example, 1.5 V+(−0.5 V)=1.0 V is applied to pin 6 (positive input) of IC14 (1/2), when the tracking servo is active. The output from pin 8 of IC14 (1/2) becomes 0 V. Just in the opposite example, if the tracking error waveform is shifted toward the negative side it operates just to offset the negative shift and no offset output is produced when the tracking servo is ON.



Part Ⓐ The diodes D29 and D31 add or subtract the threshold as below:
1.5 V+0.6 V (D29)−0.6 V (D31)=1.5 V
The 1.5 V is charged across C70.

Part Ⓑ The −0.5 V is charged across C69.

* When the unit is switched from KICK to PLAY, Q26 and Q25 turn ON, C69 −0.5 V+C70+1.5 V=1.0 V is applied to pin 6 of IC14 (1/2) and the output from pin 8 becomes 0 V.

1. CIRCUIT DESCRIPTION

1-5-11. PU DRIVE OPERATION

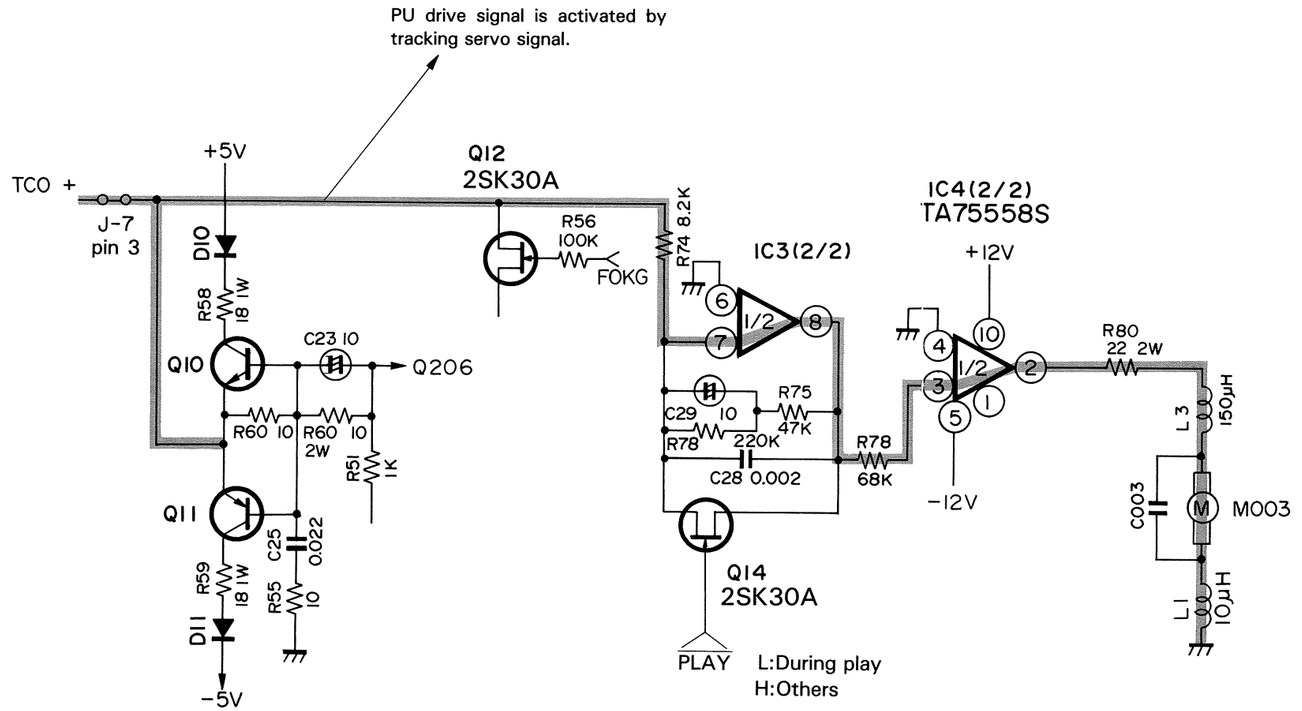


Fig. 1-5-11

Since control of the pickup feed motor should gradually be made just to compensate an offset of the tracking error signal during a normal PLAY mode, it is done by TCO+ (tracking coil+) signal only. During a normal PLAY mode, the TCO+ signal is applied to pin 7 of IC3 (2/2) through R74. Since PLAY is −12 V (pulled-down output of IC16) during normal PLAY mode, Q14 is OFF. In this state, IC3 (2/2) and RC components form a low-pass filter. As a result, the high frequency components are eliminated from TCO+ signal to obtain offset signal. It is applied to pin 3 of IC4 (2/2) through R78. After gain adjusted, it drives the pickup carry motor through R80 and L3.

1. CIRCUIT DESCRIPTION

1-5-12. FOCUS SERVO CONTROL SIGNAL OPERAITON

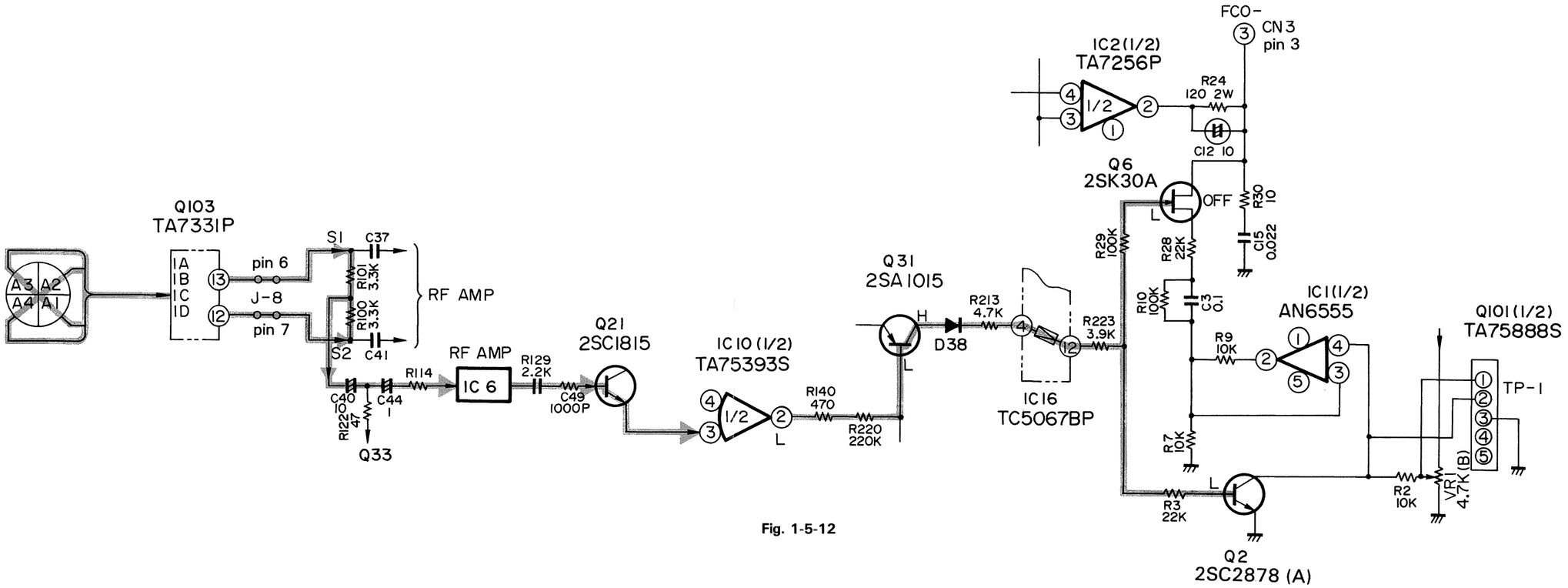


Fig. 1-5-12

1. WHEN NO DISC IS LOADED:

1. When no disc is loaded, Q6 2SK30A and Q2 2SC2878 are turned ON not to work the focus coil drive circuit, so that the focus coil can not be activated.
2. Since no signal is increased across the 4-division photodetector, no RF is available and pin 2 of IC10 (1/2) TA75393S becomes ''H'' level. The collector of Q31 2SA1015 is in turn held at a ''L'' level. It is fed to pin 4 of Inverter IC16 and pin 12 becomes ''H'' level.
3. The ''H'' level signal is applied to the gate of Q6 2SK30A through R29 100 kΩ. It turns ON to cut the signal to pin 2 of IC1 (1/2)
4. On the other hand, the ''H'' level signal is applied to the base of Q2 2SC2878 through R3 22 kΩ. Q2 is turned on to ground the FE signal. Thus, no signals are into IC1 (1/2) AN6555.
5. The switching function of Q6 and Q2 controls the operation of focus coil. It is disabled by this circuit, when no focusing is required.

2. WHEN A DISC IS LOADED AND IN PLAY MODE:

1. When a disc is loaded, a signal picked up by the 4-division photodetector is divided into two signals, S_1 and S_2 by Q103 (TA7331P). They are amplified by Q21 and fed to pin 3 of IC10 (1/2).
2. When the RF signal is present at pin 3 of IC10 (1/2), pin 2 becomes ''L'' level. It is applied to the base of Q31 (2SA1015) through R140 and R220, placing the collector of Q31 at a ''H'' level.
3. The ''H'' level signal is fed to pin 4 of IC16 through D38 and R213. Its inverted signal is available at pin 12 as an ''L'' level signal. The ''L'' level signal is then applied to the gate of Q6 (2SK30A) through R29, and Q6 is turned OFF.
4. Another signal going through R3 is applied to the base of Q2 2SC2878 turning it OFF.
   Both of Q6 and Q2 are under OFF state, the focus servo circuit works.

1. CIRCUIT DESCRIPTION

1-5-13. CONTROL SIGNAL OPERATION

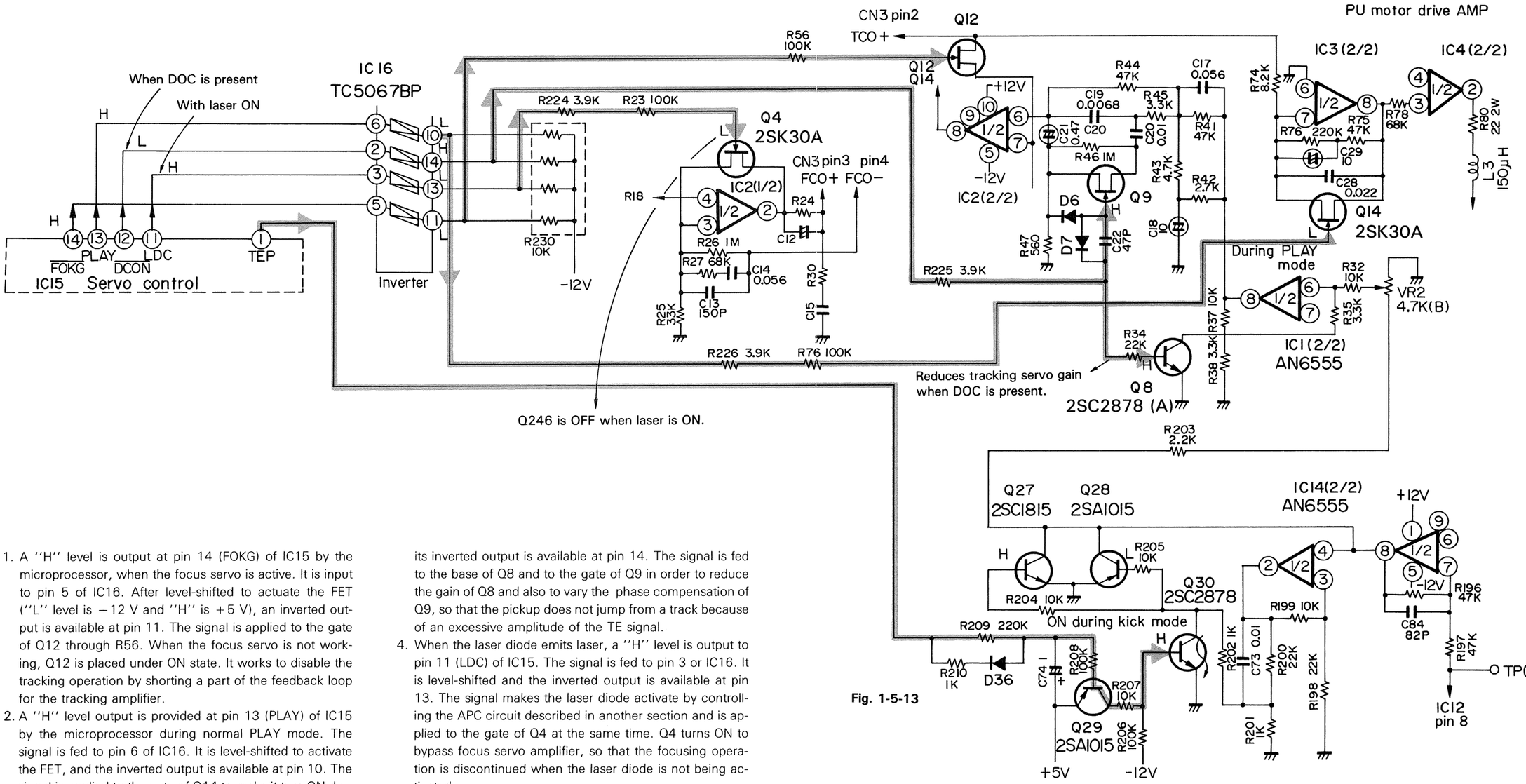


Fig. 1-5-13

1. A ''H'' level is output at pin 14 (FOKG) of IC15 by the microprocessor, when the focus servo is active. It is input to pin 5 of IC16. After level-shifted to actuate the FET (''L'' level is −12 V and ''H'' is +5 V), an inverted output is available at pin 11. The signal is applied to the gate of Q12 through R56. When the focus servo is not working, Q12 is placed under ON state. It works to disable the tracking operation by shorting a part of the feedback loop for the tracking amplifier.
2. A ''H'' level output is provided at pin 13 (PLAY) of IC15 by the microprocessor during normal PLAY mode. The signal is fed to pin 6 of IC16. It is level-shifted to activate the FET, and the inverted output is available at pin 10. The signal is applied to the gate of Q14 to make it turn ON during the modes other than PLAY. This bypasses the pickup carry motor amp and prevents the tracking error signal from driving the pickup feed motor.
3. When an RF signal drops out for a certain period of time because of scratches or dusts on a disc, a dropout detection signal of ''L'' level is provided at pin 12 (DCON) of IC15 at the same spot per every revolution of the disc. The signal is applied to pin 2 of IC16. It is level-shifted, and its inverted output is available at pin 14. The signal is fed to the base of Q8 and to the gate of Q9 in order to reduce the gain of Q8 and also to vary the phase compensation of Q9, so that the pickup does not jump from a track because of an excessive amplitude of the TE signal.
4. When the laser diode emits laser, a ''H'' level is output to pin 11 (LDC) of IC15. The signal is fed to pin 3 or IC16. It is level-shifted and the inverted output is available at pin 13. The signal makes the laser diode activate by controlling the APC circuit described in another section and is applied to the gate of Q4 at the same time. Q4 turns ON to bypass focus servo amplifier, so that the focusing operation is discontinued when the laser diode is not being activated.
5. A ''H'' level output is applied to pin 1 (TEP) of IC15 only during normal PLAY mode. It, however, becomes ''L'' level, when a kick signal is given during the normal PLAY mode. The signal is integrated by R210, R209, D36 and C74 to turn on Q29 and Q30. In this instance, Q27 and Q28 are placed under OFF condition by making Q30 turn ON during the kick mode. The noise limiter circuit is thus disabled during search mode.

1. CIRCUIT DESCRIPTION

1-5-14. SERVO CONTROL CIRCUIT OPERAITON

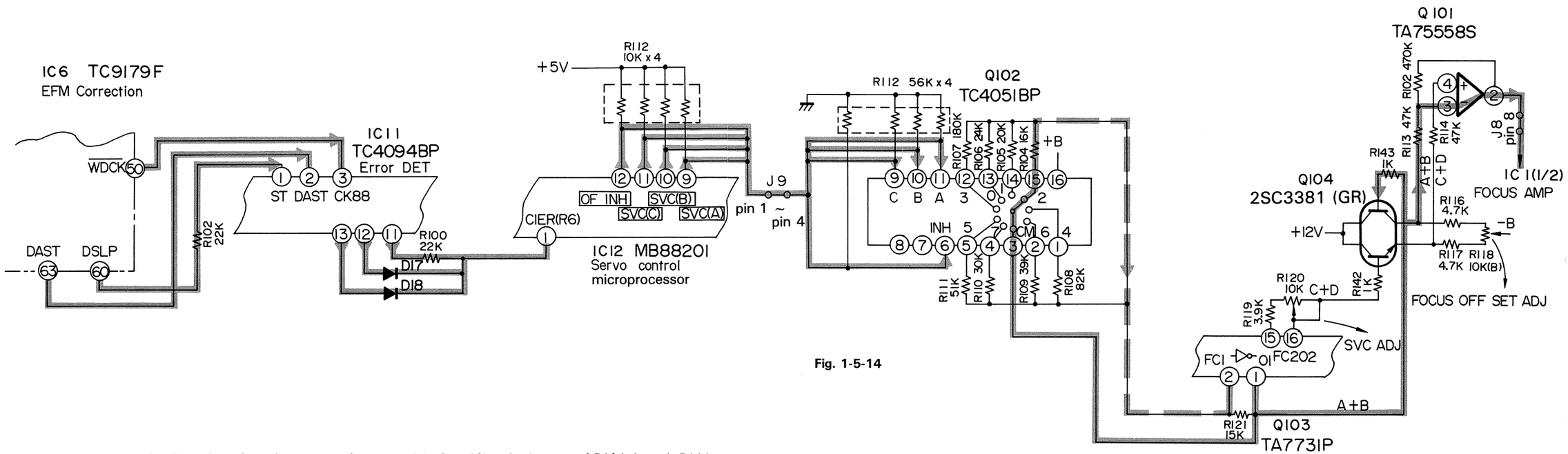


Fig. 1-5-14

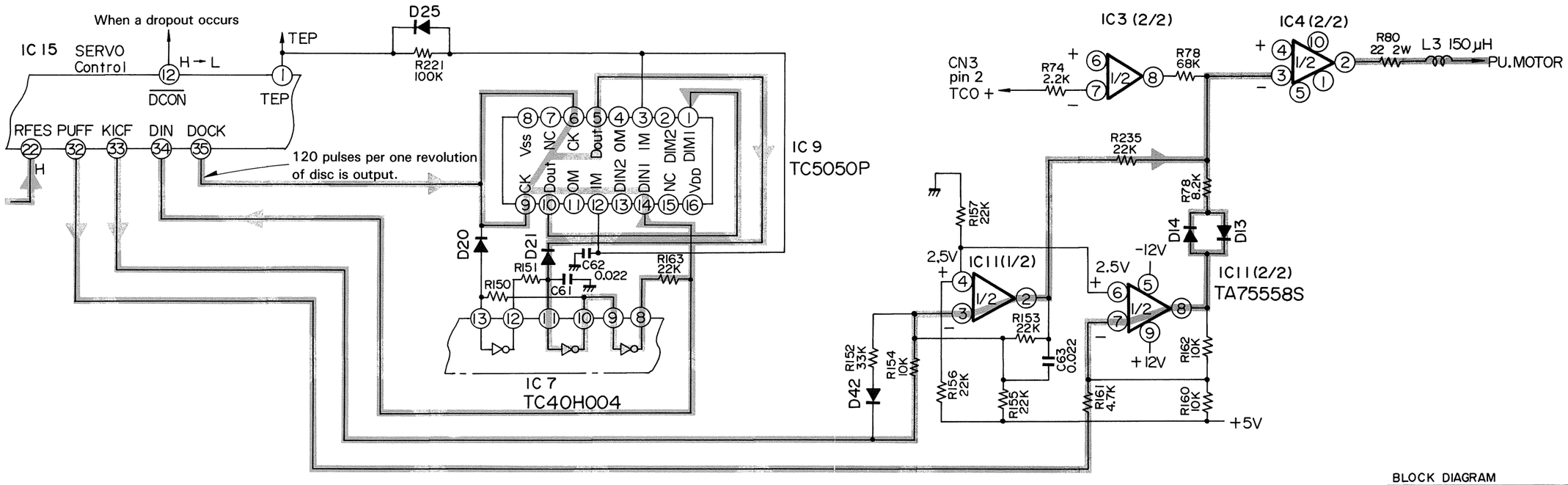
1. The focus error signal is figured out from the outputs of 4-division photodetector under operational processing (A + B) − (C + D). Outputs (A + B) and (C + D) must have a proper balance, otherwise no adequate sevo operation is possible. The optimum balance varies depending on a disc and ambient environment and has no absolute value. The balance adjustment is automatically made everytime when a disc is changed or switched from the STOP mode to the PLAY mode. This is called SVC (servo control). The operating principle of the circuit is to adjust to an optimum one out of the 9-step predetermined balances using the error number in the EFM signal.
2. C_1 and C_2 error detection conditions (''H'' level when an error occurs) in the EFM signal is output to pin 63 (DAST) of IC6 (TC9179F). A clock signal of 88.2 kHz, which indicates one word output period, is made available at pin 50 (WDCK) and a frame latch pulse signal, which indicates one frame, is available at pin 60 (DSLP). These three signals are coupled to a shift register with strobe function IC11 (TC4094BP). DAST (error present) is input as data, WDCK as shift clock and DSLP as strobe signal. As a result, C_1 error presence condition per every one frame is output at pin 11 to 13 of IC11. They are then applied to pin 1 of IC12 (MB88201) through a wired OR circuit (''H'' level indicates the error detection.)
3. 4-bit Microprocessor IC12 (MB88201) counts the error number in the EFM signal at pin 1 and controls 8-channel multiplexer Q102 (TC4051BP) via four ports (pin 9 to 12), selecting one of R104 through R111 connections, which are placed in parallel with R121 connected to pin 1 and 2 of Q103 (TA7731P). (Refer to the truth table at right showing the connection status.)
4. The 4-division photodetector signal (A + B) is output to pin 1 of Q103. Pin 2 is used as a feedback terminal for the last stage amplifier. In the same way, the (C + D) signal is available at pin 16 and 15 is a feedback terminal. R121 is a feedback resistor to determine the output level at pin 1 of (A + B) signal. When one of R107 through R111 is connected in parallel, the ouptut level varies. R119 and R120 are feedback resistors to determine the ouptut level (pin 16) of the (C + D) signal and R120 is a trimming potentiometer to adjust the initial condition of SVC.
5. The (A + B) signal and the (C + D) signal are applied to the bases of Q104 respectively and their differences appear at the emitters. The voltage difference between the emitters is expressed as (A + B) − (C + D). It is applied to pin 3 and 4 of Q101. After amplified, it is used as a focus error signal. R118 in this circuit adjusts the DC offset of the focus error signal when no signals are being received.
6. As described above, 4-bit microprocessor IC12 determines an optimum balance (approximately minimum of the error number) of the focus error signal (A + B) − (C + D), changing the output level of (A + B) to nine steps by automatically switching the feedback resistance for the (A + B) signal depending on the error number.
7. The pickup has an offset amount in the focusing direction. Therefore, the optimum focusing point is looked for by use of an exclusive microprocessor (IC12). Moreover, when PLAY is made from the tray open state or the stop mode, the microprocessor varies the resistance value between pins 1 and 2 of Q103 by switching bilateral switches in the 8-channel multiplexer IC (Q102) to select a resistance value at which error is suppressed.
8. For example, when the microprocessor indicates (INH, A, B C) = (L, L, L, L), pin 13 of Q102 is connected to pin 3 of Q102. Thus, 24 kΩ resistance is connected in parallel with the 15 kΩ resistance already inserted between pins 1 and 2 of Q103, so that the resistance value between pins 1 and 2 is 9.23 kΩ.

Q102 pin No.	Q102 input INH	Q102 input A	Q102 input B	Q102 input C	PU alignment level	Resistance	Resistance value between pins 1 and 2 of Q103
6	H	L	L	L	INH	∞	15 k
12	L	H	H	L	3	180 k	13.8 k
1	L	L	L	H	4	82 k	12.7 k
5	L	H	L	H	5	51 k	11.6 k
2	L	L	H	H	6	39 k	10.8 k
4	L	H	H	H	7	30 k	10 k
13	L	L	L	L	0	24 k	9.23 k
14	L	H	L	L	1	20 k	8.57 k
15	L	L	H	L	2	16 k	7.74 k

Table 1-5-14 Select a resistance value of SVC

1. CIRCUIT DESCRIPTION

1-5-15. DROPOUT POSITION DETECTION OPERATION AND PUFF, KICF OPERATION

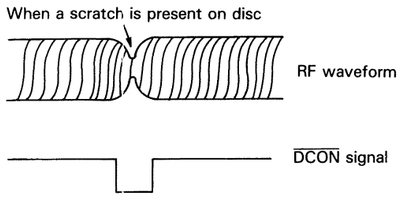


BLOCK DIAGRAM

FIG. 1-5-15

Detection of Dropout Position

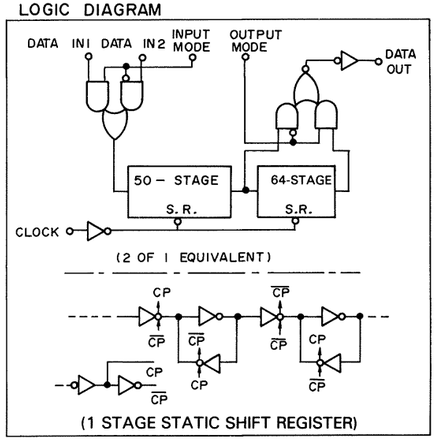
1. The dropout control circuit employed in this unit has been designed to be strong against scratches or shocks. The FGS signal (20 pulses generated per one revolution of the disc motor) is applied to pin 39 (FGS) of IC15 (TC15G or T7001) and it is 6 times frequency multiplied internally. An output with 120 pulses per one revolution is output to pin 35 (DOCK). If a scratch is present, the number of pulses are counted. The level at pin 12 (DCON) of IC15 is switched from "H" to "L" at the same position where the scratch was present but one track behind. Q8 and Q9 in the tracking servo circuit are turned ON to increase the gain of the tracking servo control. Thus, the system is protected against scratches or shocks.
2. If a scratch is found on the surface of a disc, pin 8 (RFES) of comparator IC10 (2/2) is switched from "L" level to "H" level and pin 22 of IC15 turns to "H" level. When pin 22 becomes "H" level, a shift register is set inside IC15 and the DOCK signal (120 pulses per one revolution of disc) is counted. Both of the shift register inside IC15 and external register IC9 are used for the counting purpose. When the 120 pulses are counted, the output is available at pin 5 (D_{OUT}) of IC9 and it is fed to pin 11 of IC7. Its output is obtained from pin 8 and it is fed to pin 34 (DIN) of IC15. This changes the level at pin 12 ($\overline{DCON}$) from "H" to "L".
3. Tracking error pulse control signal is present at pin 1 (TEP) of IC15 and it is "H" level during the normal PLAY mode. It, however, switches to "L" level during KICK mode. This is input to pin 3 and 12 of IC9 to disable the circuit during that mode.

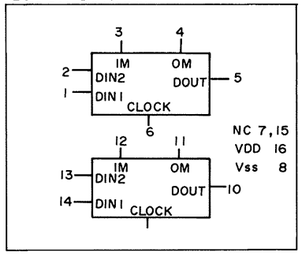


Dropout position detection

TC-5050P (Shift Registor)

LOGIC DIAGRAM

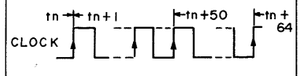




TRUTH TABLE

tn , tn+1			tn+50		tn+64	
DIN1	DIN2	IM	OM	DOUT	OM	DOUT
H	※	H	L	H	H	H
L	※	H	L	L	H	L
※	H	L	L	H	H	H
※	L	L	L	L	H	L

※ Don't Care



(used as 114 bit shift register)

1. CIRCUIT DESCRIPTION

PUFF, KICF

1. This is a circuit to control the carry motor for the pickup. During normal PLAY mode, the pickup carry motor can be controlled only by the TCO + signal, just to compensate the offset of the tracking error signal. During SEARCH or FAST FORWARD (FF, REV) mode, however, it has to be moved more quickly. For this reason, the movement is controlled by KICF and PUFF.
2. More precisely, during a long (far) SEARCH mode, PUFF is used and during a short (close) SEARCH, FAST FORWARD or PAUSE mode, KICF is used for the control purpose.
3. KICF (available at pin 32 of IC15) is high impedance during the normal PLAY mode. The input voltage at pin 3 of IC11 (1/2) becomes 2.5 V by R153 and R155. Since the input voltage at pin 4 of IC11 (1/2) is set at 2.5 V by R157 and R156, the output from pin 2 of IC11 (1/2) becomes 0 V.
4. PUFF (available t pin 33 of IC15) is also high impedance during the normal PLAY mode. The input at pin 7 of IC11 (2/2) becomes 2.5 V by R160 and R162. Since the input voltage at pin 6 of IC11 (2/2) is set at 2.5 V, the output at pin 8 becomes 0 V.
5. When the pickup is moved in the FORWARD (FF) direction, PUFF and KICF are "H" level. Inverted input pin 7 and 3 of IC11 are "H" level and output at pin 8 and 2 are at "L" level. Inverted input pin 3 of IC4 (2/2) is also at "L" level to provide the carry motor with a high revolution in the clockwise direction.
6. When the pickup is moved in the BACKWARD (REV) direction, both of the PUFF and KICF are "L" level. By making the input of Q214 "L" level and the output "H" level, the carry motor can be revolved at a high speed in the counterclockwise direction.

Mode / Signal	Normal PLAY	Long Search (More than 512 tracks)		Short Search (Less than 512 tracks)		FF	REV
		FF Direction	REV Direction	FF Direction	REV Direction		
KICF	2.5V	2.5	2.5	5 / 2.5 / 0	5 / 2.5 / 0	5 / 2.5 / 0	5 / 2.5 / 0
PUFF	2.5V	5	0	2.5	2.5	2.5	2.5

Control Signal during each Mode

Applies reverse voltage to put a brake.

Unit [V]

1. CIRCUIT DESCRIPTION

1-5-16. KEY DATA AND TIMING PULSE OPERATION

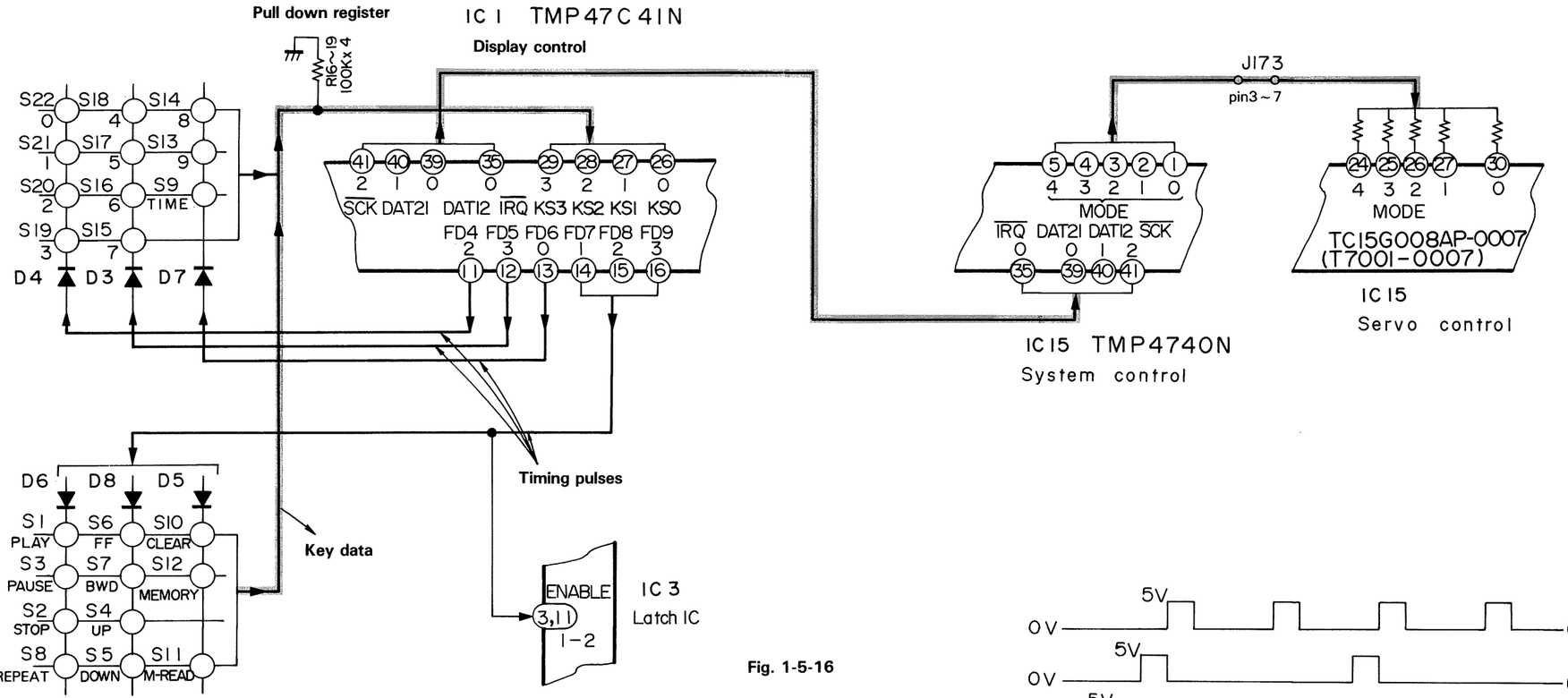


Fig. 1-5-16

1. Since the unit has many function keys, a 6 x 4 matrix had been made in order to make the best use of the input/output ports of IC1 (4-bit microprocessor). The key input can be judged by key scanning pulses from IC1 (6 lines in time division) and four key input lines.

2. Pin 11 to 16 of IC1 are periodically providing the pulses staggered by a regular timing as shown. Each of them enters the vertical line of the key matrix through a diode, which prevents more than 2 keys from being pressed at the same time. Pin 26 to 29 are input lines and they are all 0 V when no keys are pressed.
   For example, when the PLAY key is pressed. The pin 14 line and pin 26 are shorted, and scanning pulse from pin 14 is input to pin 26.
   IC1 (4-bit microprocessor) recognizes that the PLAY key has been pressed, based on the input to pin 26 and the timing of pulse at pin 14 and gives the PLAY instruction to IC15 (control microprocessor.)
   The reason that the timing pulse has a double frequency at pin 16 is that two clock signals are entered simultaneously, when M-READ and CLEAR keys are pressed at same time.

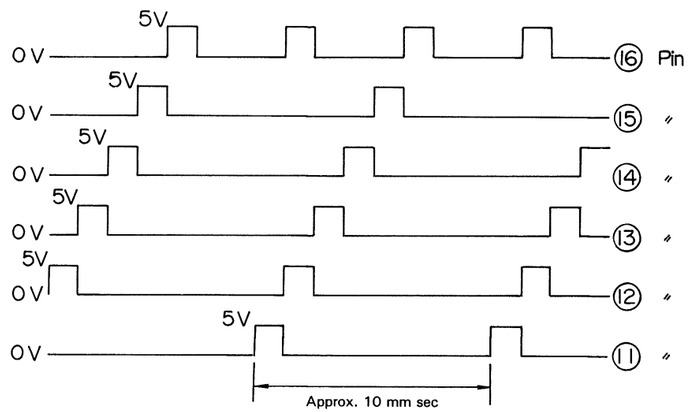


Fig. 1-5-16-2 IC1 Timing Pulse Waveform

1. CIRCUIT DESCRIPTION

1-5-17. EFMI SIGNAL CIRCUIT OPERATION

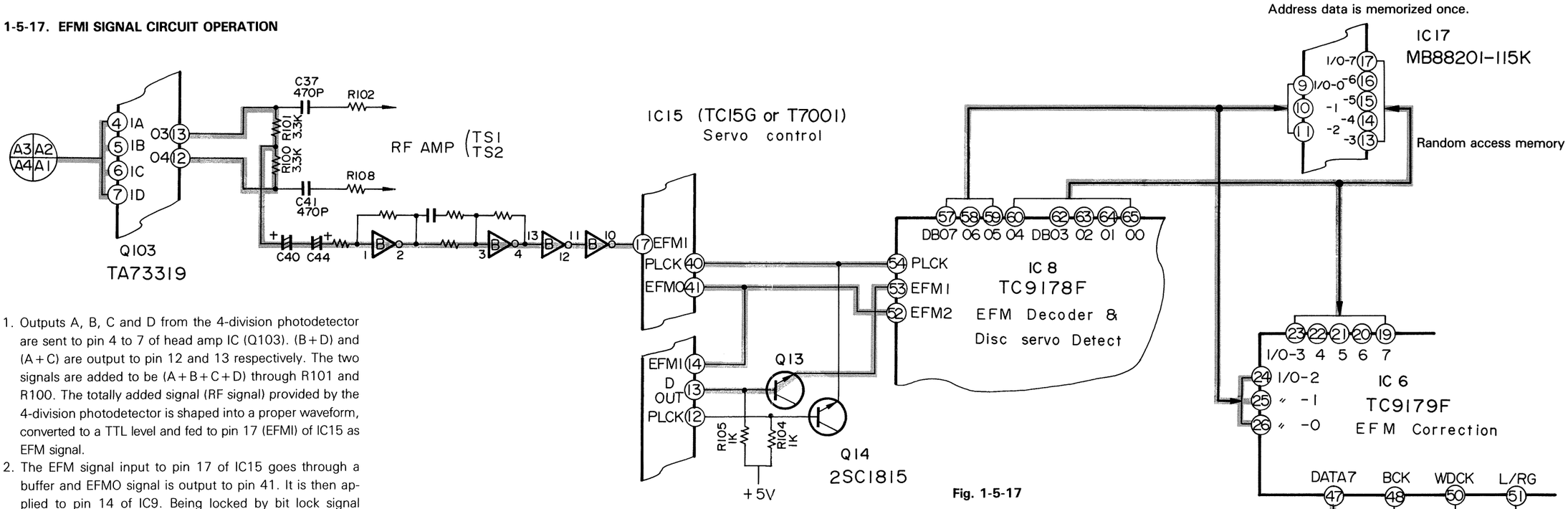


Fig. 1-5-17

1. Outputs A, B, C and D from the 4-division photodetector are sent to pin 4 to 7 of head amp IC (Q103). (B+D) and (A+C) are output to pin 12 and 13 respectively. The two signals are added to be (A+B+C+D) through R101 and R100. The totally added signal (RF signal) provided by the 4-division photodetector is shaped into a proper waveform, converted to a TTL level and fed to pin 17 (EFMI) of IC15 as EFM signal.
2. The EFM signal input to pin 17 of IC15 goes through a buffer and EFMO signal is output to pin 41. It is then applied to pin 14 of IC9. Being locked by bit lock signal (PLCK), DOUT signal with its jitter component eliminated is produced. (Refer to section 1-5-18. PLL CIRCUIT OPERATION.)
   The EFMI, PLCK and DOUT signals are fed to IC8 (TC9178F) and processed.
3. 14-bit 1 symbol is converted to 8-bit 1 symbol, using the EFM signal fed to pin 53 of IC8. The 8-bit outputs are provided at pin 57 to 65. The 8-bit data is once memorized in IC17 (RAM). After being delayed by necessary number and jitter absorbed inside IC17, it is read out for IC6 (TC9179F). Inside IC6, C1 error pattern is first produced to correct the error symbol data.
4. Next, each data of every symbol is again read out by IC6 to correct the C2 error, after being properly delayed for the processing de-interleave. The processed data is finally sent from IC17 to IC6, where the data, which was impossible to correct, is average compensated. The output is available at pin 47 as a serial 16-bit data alternately for the Lch and Rch.
5. L and R alternating 16-bit serial data signal and clock (BCLK, LRCK, WCLK) signal are originally sent from IC6 (BCK, L/RG, $\overline{\text{WDCK}}$ respectively). BCLK is 1.411 MHz, LRCK is 44.1 kHz and WCLK is 2 x LRCK (88.2 kHz), logic signal respectively. The BCLK signal is applied to pin 9 of IC21. The WCLK, DIN, BCLK and LRCK signals are applied to pin 10, 8, 9 and 7 of IC21 respectively. The data WCLK, DIN and LRCK is synchronized with the rising edge of the BCLK signal being applied to pin 9.
6. The integral current output of IC21 appear at pin 17 (IOUTR) and pin 18 (IOUTL), and at the same time are level-shifted by VR2 and VR3 connected to pin 1 of IC23 and pin 7 of IC22 respectively (DC offset adjustment).
   In IC24 and 25, the L and R signals of the integrator outputs are selected by applying an L/R switching pulse (LRCK OUT 11 of IC21). The Lch and Rch output signals are output to pin 3 and 5 respectively. IC22, 23 are a simple low-pass filter to shape the waveforms, which are put into LPF1 and LPF2 respectively.
7. LPF1 and LPF2 eliminate unwanted frequencies beyond 20 kHz outside the audio frequency range and required audio signals are available at the Lch output and the Rch output respectively. The signals are applied to pin 3 and 5 of buffer amp IC27 (also works as an emphasis ON/OFF switch. Refer to section 1-5-21.) through resistors and their outputs are provided at pin 1 and 7. A part of the outputs is directly connected to FIXED OUTPUT and the other is fed to buffer amp IC19 through VR1 (on the front panel) and output to pin 1 and 7 for headphones.

1. CIRCUIT DESCRIPTION

1-5-18. PLL CIRCUIT OPERATION

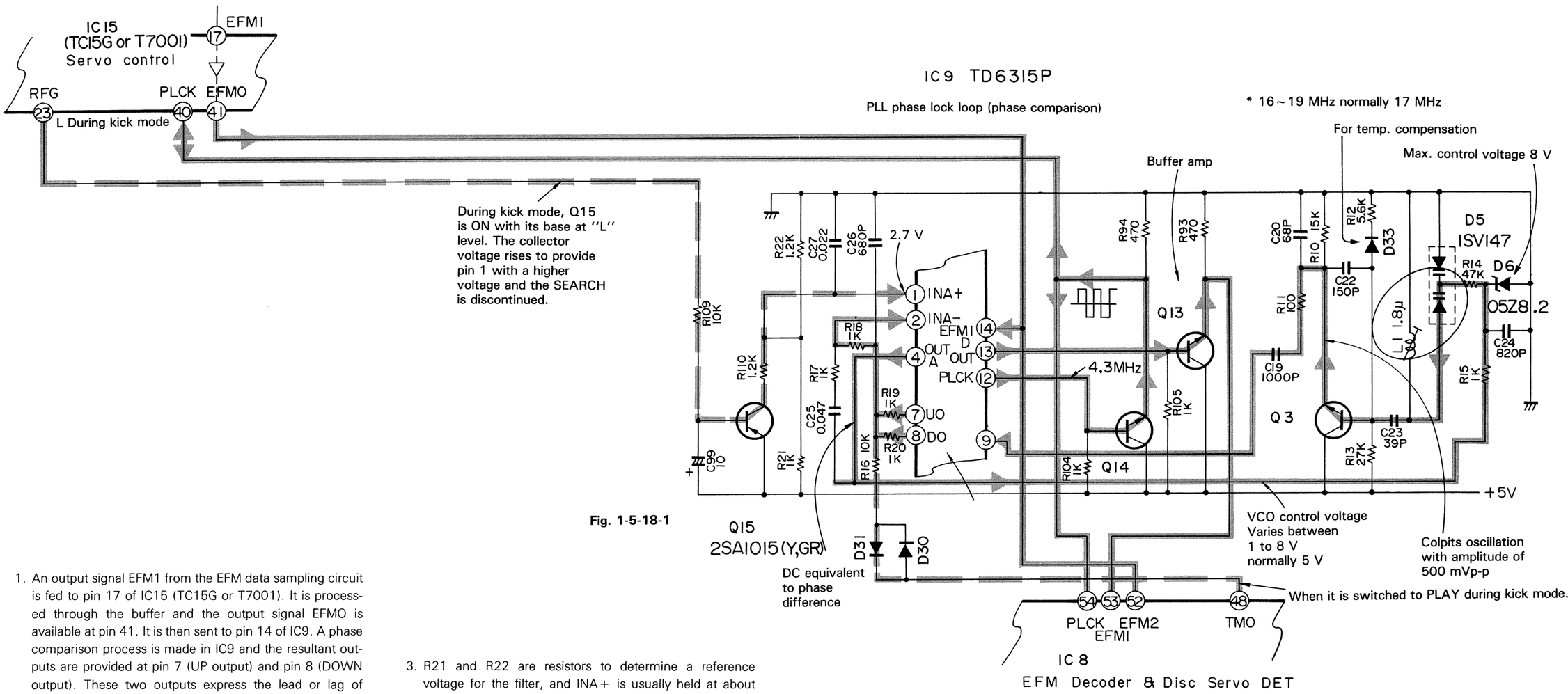


Fig. 1-5-18-1

1. An output signal EFM1 from the EFM data sampling circuit is fed to pin 17 of IC15 (TC15G or T7001). It is processed through the buffer and the output signal EFMO is available at pin 41. It is then sent to pin 14 of IC9. A phase comparison process is made in IC9 and the resultant outputs are provided at pin 7 (UP output) and pin 8 (DOWN output). These two outputs express the lead or lag of phase between the EFM signal and bit clock signal (PLCK). When a frequency of the PLCK is lower than the EFM clock, pin 7 is held at "L" level for a longer time, decreasing the period of high impedance. On the contrary pin 8 becomes "H" level for a shorter period of time and the period of high impedance is increased.
2. The UP and DOWN outputs are added through R20 and R19, and fed to a low-pass filter. Comparing it with a reference voltage, the phase difference is applied to VCO as DC output. An operation amp for the low-pass filter purpose is built in IC9, pin 1 (INA+) is for non inverted input and pin 2 (INA−) is for inverted input respectively. pin 4 is an output terminal. The added UP and DOWN output is fed to INA− through R18. R17 and C25 form a filter network.
3. R21 and R22 are resistors to determine a reference voltage for the filter, and INA+ is usually held at about 2.7 V. During the SEARCH mode, however, the reference voltage is raised up (about 3 V) to shorten the search period. For this purpose, an RFG signal of "L" level is applied to the base of Q15 to turn it ON and its "H" output is added to INA+ through R110 during the SEARCH period.
4. The output from pin 4 (OUTA) of low-pass filter output controls voltage for VCO through R15. The VCO has been designed to oscillate at about 16 MHz to 19 MHz with a control voltage range of 1 V to 8 V. Under normal PLAY condition, it is oscillating at about 17 MHz with a control voltage of about 5 V. D6 is a zener diode to limit the control voltage at a maximum of 8 V and D5 is a variable capacitance diode. It forms a colpitts oscillator together with L1. R12 and R13 provide a bias to Q3 and D33 is a temperature compensation diode.
5. An oscillation amplitude of VCO is about 500 mVp-p. Eliminating the DC component by C19, it is applied to pin 9 of IC9. Being amplified in IC9 and 1/4 frequency divided, the output is available at pin 12 as PLCK. (The PLCK is about 4.3 kHz during normal PLAY mode.) EFMI input to pin 14 is synchronized by the PLCK, and the DOUT output is available at pin 13. Q14 and Q13 are connected in an emitter follower configuration and work as a buffer for the PLCK and DOUT signals. If the waveform of EFMI, PLCK and DOUT signals are observed with the PLL circuit at the normal PLAY condition, the clean waveform is locked as shown in the diagram at right.

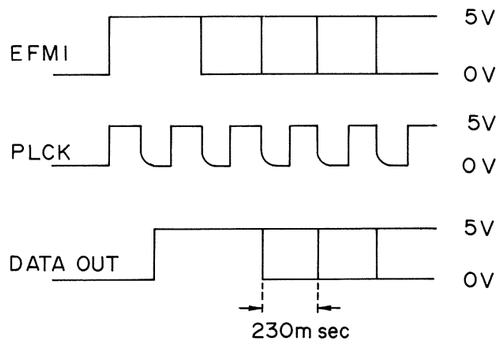


Fig. 1-5-18-2 PLL Timing Relationship

1. CIRCUIT DESCRIPTION

1-5-19. MUTING CIRCUIT OPERATION

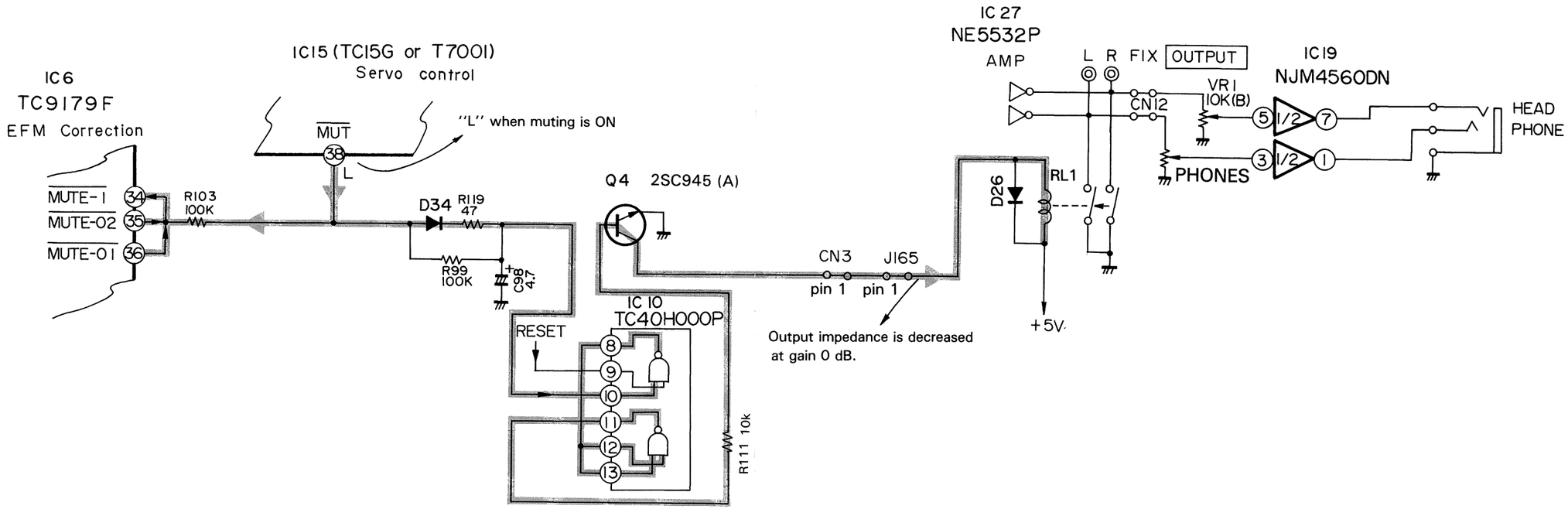


Fig. 1-5-19

1. There are following two cases where muting output is required. One is during all modes except the normal PLAY mode, and the other is when adequate correction or compensation for normal playback can not be secured because of too many errors contained in the EFM signal depending on the condition of a disc even if it is normally being played. The muting can be made by the following two methods. One method is to mute the last output stage of the analog signal by using a relay and the other is to turn OFF the 16-bit digital signal in the process circuit. For this reason, the former is called analog muting and the latter is called digital muting.
2. Pin 38 of IC15 (TC15G or T7001) is at "L" level during all modes except normal PLAY mode and it provides 0 V to the base of Q4. Q4 is turned OFF, making relay RL1 OFF. The output is thus muted. At the same time, pin 34 of IC6 (TC9179F) is also held at "L" level through R103. The output of 16-bit digital signal is turned OFF inside IC6.
3. When bad conditions of a disc (scratches or dust) make the adequate correction and compensation impossible because of too many errors in the EFM signal even during normal PLAY mode, pin 35 and 36 become "L" level. Pin 34 of IC6 turns to "L" level by a wired OR connection. The digital muting is thus accomplished by turning the 16-bit digital signal OFF.

1. CIRCUIT DESCRIPTION

1-5-20. REMOTE CIRCUIT OPERATION
(TRANSMITTER HAS A SIMILAR OPERATION AS TV OR VIDEO AND WILL NOT BE EXPLAINED)

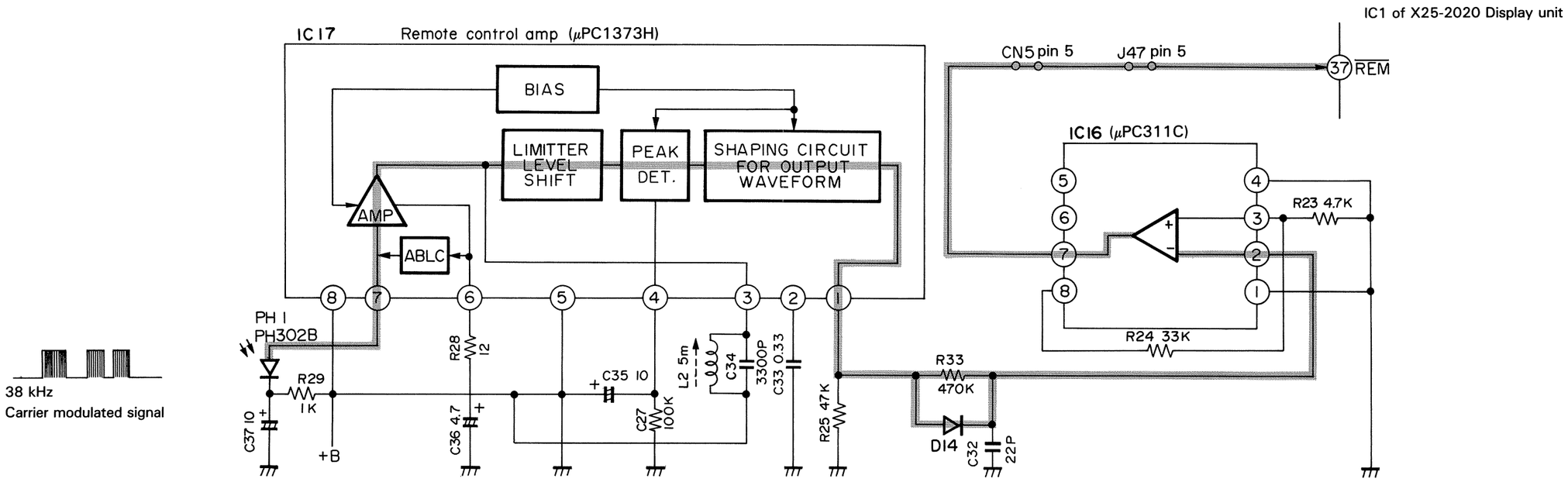
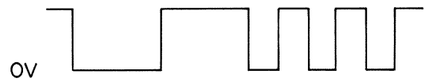


Fig. 1-5-20

1. A data signal (modulated by a 38 kHz carrier) sent from the transmitter enters to infrared ray sensor diode PH1. PH1 varies the current through it by changing its internal resistance in accordance with the input signal. The quiescent point current is determined by load resistor R29 and +B supply. The varying current signal is fed to pin 7 of remoto control amp IC17. It is about 40 dB amplified here and the output is available at pin 1.
2. The signal is fed again to pin 2 of IC16 through the detection circuit of D14, amplification centering around 38 kHz. The output appears at pin 7. The signal waveform-shaped by IC16 as shown at right is fed to pin 37 of IC1 for the control purpose of the microprocessor.

38kHz carrier
Transmitted waveform



Output waveform of receiver circuit
(Input at pin 37 of IC1 (TMP47C40N))

1. CIRCUIT DESCRIPTION

1-5-21. EMPHASIS CIRCUIT OPERATION

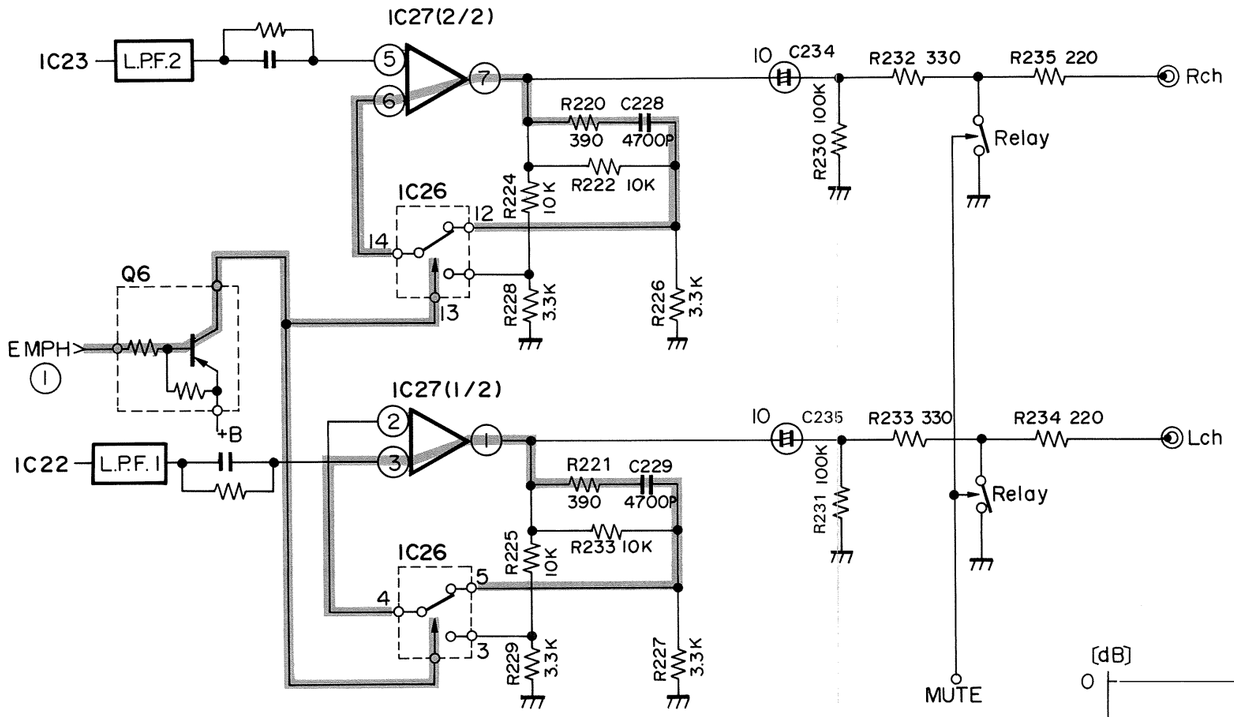


Fig. 1-5-21-1

1. When playing a disc, the level in the high frequency range can be lowered to the same degree as when the disc has been recorded with its high frequency level enhanced in order to improve the high frequency characteristic. The procedure to enhance is called emphasis. If a disc has been emphasized, its information has been included in the subcode data of the disc.
   (To lower the high frequency level during PLAY mode is called de-emphasis.)
2. PROCESS IC8 (TC9178F) outputs pin "H" level at pin 12 by reproducing and decoding EFM signal, if the playing disc is an emphasized one. The signal is sent to the base of Q6. R220+C228, R221+C229 are high frequency damper elements. When Q6 turns OFF, the frequency characteristic of the amplifier changes to be a response curve with its high-end cut as shown to provide the de-emphasis.

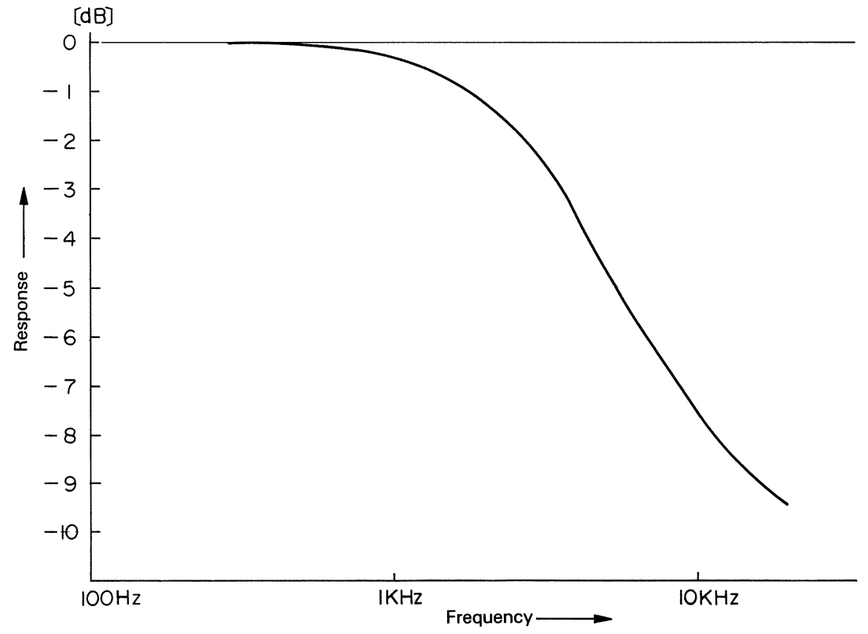


Fig. 1-5-21-2 Frequency response of high-end cut.

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-1 Head amp (J25-4404-08)

2-1-1 Q103 (TA7731P) head amp

Q103 (TA7731P) is the head amp and operation IC for the laser beam receiver device, developed for CD system DAD player.

Pin connection diagram

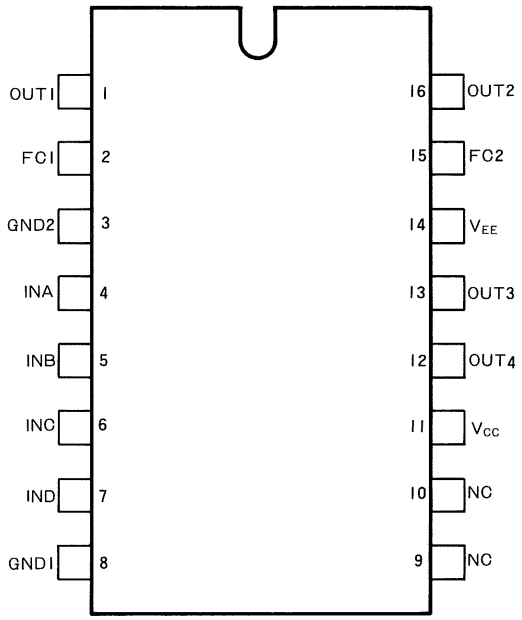


Fig. 2-1A

Block diagram

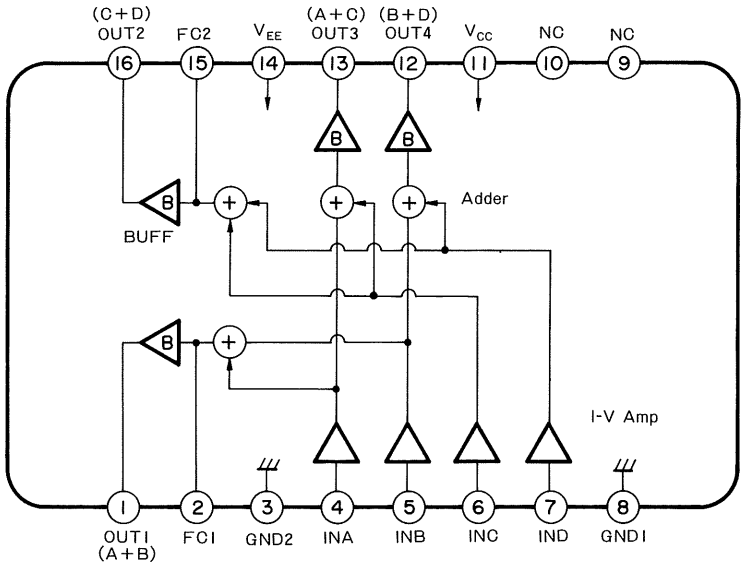


Fig. 2-1B

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin functions

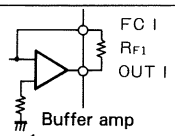
Pin No.	Symbol	Description	Remarks
1	OUT1	Pin which outputs the sum signal (A + B) of pin IN A and IN B input signals out of 4-division photodetector outputs. The final stage buffer amp is provided with an external feedback resistance to neutralize the effect of the irregularity in characteristics between photodiodes.	 Note 1 With max. input of 100 kHz ...Transfer impedance = 27 kΩ R_{F1} = 9 kΩ (typical)
2	FC1	Final stage buffer amp negative input pin of OUT1 output signal. A resistance is connected between this pin and pin OUT1 to control the gain.	
3	GND2	GND pin	
4	IN A	Input pin of signal A (one of 4-division photodetector outputs)	Note 1
5	IN B	Input pin of signal B (one of 4-division photodetector outputs)	
6	IN C	Input pin of signal C (one of 4-division photodetector outputs)	
7	IN D	Input pin of signal D (one of 4-division photodetector outputs)	
8	GND1	GND pin	
9-10	NC	Not connected	
11	V_{CC}	Positive supply voltage pin	
12	OUT4	Pin which outputs the sum signal (B + D) of pin IN B and IN D input signals out of 4-division photodetector outputs.	
13	OUT3	Pin which outputs the sum signal (A + C) of pin IN A and IN C input signals out of 4-division photodetector outputs.	Note 1 With max. input of 100 kHz ...Transfer impedance = 27 kΩ (typical)
14	V_{EE}	Negative supply voltage pin	
15	FC2	Final stage buffer amp negative input pin of OUT2 output signal. A resistance (for feedback) is connected between this pin and pin OUT2 to control the gain.	

Table 2-1A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

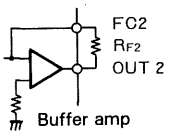
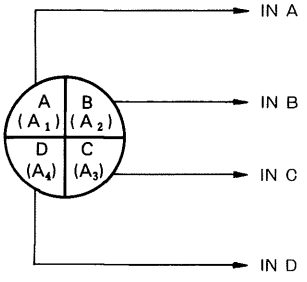
Pin No.	Symbol	Description	Remarks
16	OUT2	Pin which outputs the sum signal (C + D) of pin IN C and IN D input signals out of 4-division photodetector outputs. The final stage buffer amp is provided with an external feedback resistance to neutralize the effect of the irregularity in characteristics between photodiodes.	 Note 1 With max. input of 100 kHz ...Transfer impedance = 27 kΩ R_{F1} = 9kΩ

Table 2-1A

Note 1: 4-division photodetector configuration



2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-1-2 Q102 (TC4051BP) SVC switch

TC4051BP, of 8-channel configuration, is a multiplexer capable of selecting analog or digital signal, or combining them. The switch pin corresponding to each channel turns ON with the digital signal from the control pin.

Truth table

CONTROL INPUTS				"ON" CHANNEL
INHIBIT	C	B	A	TC4051BP
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7

Table 2-1C

Block diagram

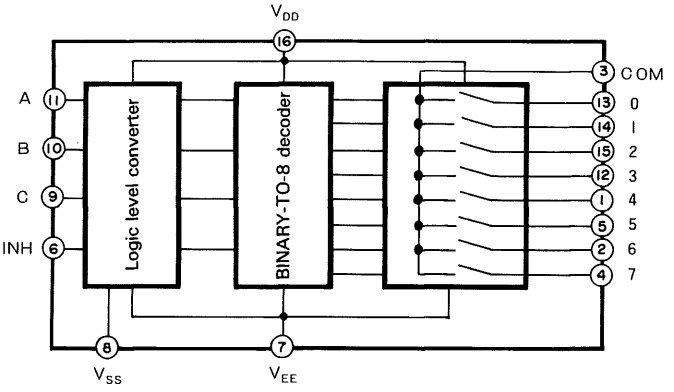


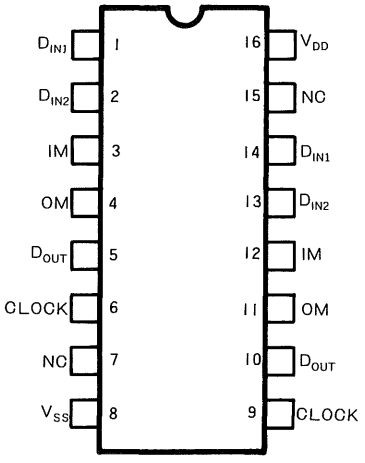
Fig. 2-1D

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

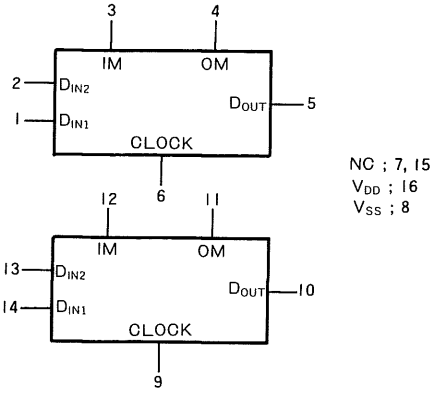
2-2 Servo board (X29-1520-00)

2-2-1 IC9 (TC5050P) dropout memory, 50-stage/114-stage selection type shift register

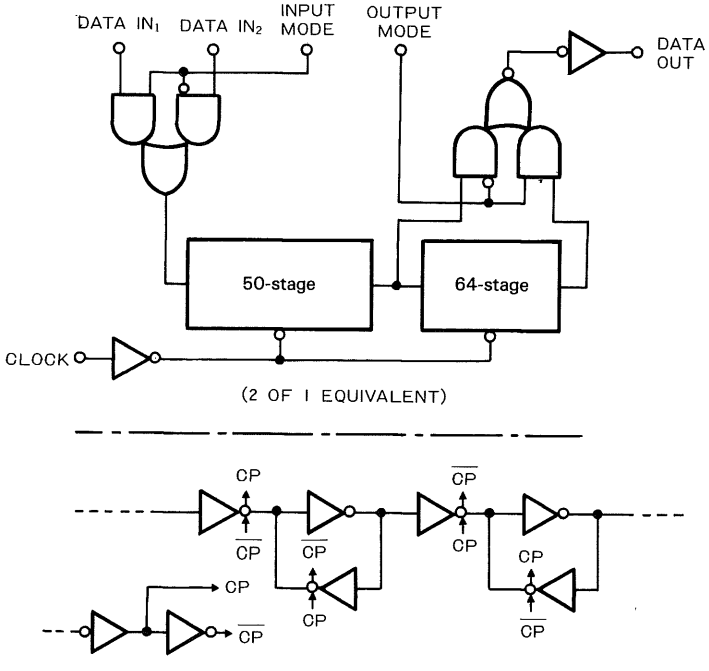
Pin connection diagram



Block diagram

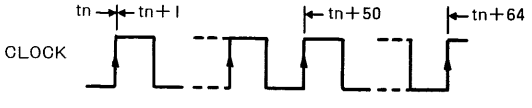


Logic diagram



Truth table

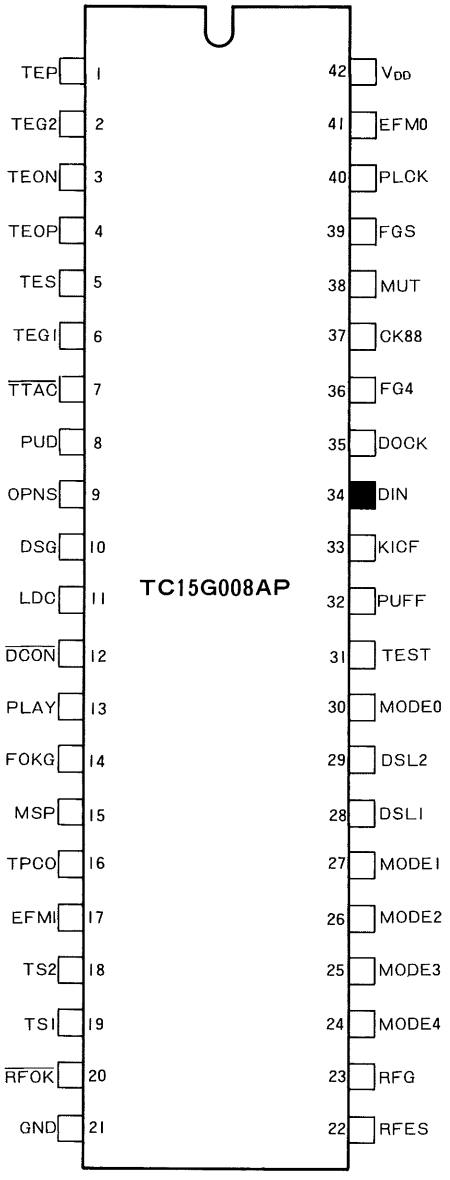
t_n, t_{n+1}			t_{n+50}		t_{n+64}	
D_{IN1}	D_{IN2}	IM	OM	D_{OUT}	OM	D_{OUT}
H	*	H	L	H	H	H
L	*	H	L	L	H	L
*	H	L	L	H	H	H
*	L	L	L	L	H	L



2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-2-2 IC15 (TC15G008AP) semi-custom IC

Pin connection



■ ; I/O port

Fig. 2-2-2A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Block diagram

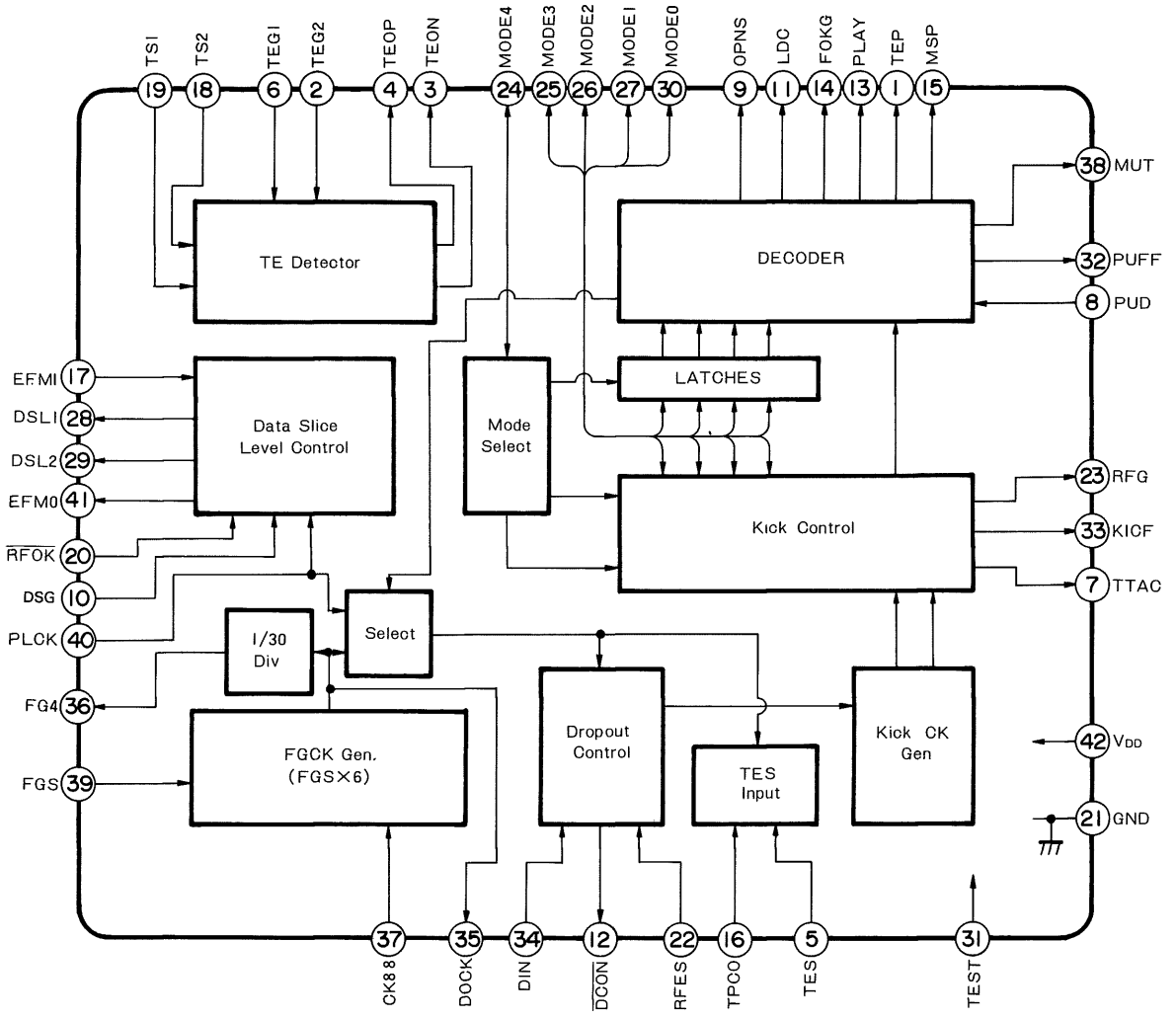


Fig. 2-2-2B Internal block diagram

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin functions

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin name</th><th>IN/OUT</th><th>Description</th><th>Remarks</th></tr>
<tr><td>1</td><td>TEP</td><td>Tracking error pulse control output</td><td>O</td><td>Outputs a "H" signal only during play. However, it becomes "L" when the kick signal is output during play.</td><td></td></tr>
<tr><td>2</td><td>TEG2</td><td>Tracking error detector control (1) input</td><td rowspan="2">I</td><td rowspan="2"><table><tr><th>TEG1</th><th>TEG2</th><th>Function</th></tr><tr><td>H</td><td>H</td><td>Tracking error detection and normal operation</td></tr><tr><td>L</td><td>H</td><td>TEOP outputs a "H" signal at the timing of the absolute phase difference between TS1 and TS2.
TEON is fixed to "H".</td></tr><tr><td>H</td><td>L</td><td>TEON outputs a "L" signal at the timing of the absolute phase difference between TS1 and TS2.
TEOP is fixed to "L".</td></tr><tr><td>L</td><td>L</td><td>Stop of tracking error detection. TEOP is fixed to "L".
TEON is fixed to "H".</td></tr></table></td><td rowspan="2">Pullup resistor incorporated</td></tr>
<tr><td>6</td><td>TEG1</td><td>Tracking error detector control (2) input</td></tr>
<tr><td>3</td><td>TEON</td><td>Tracking error negative output</td><td>O</td><td>When TS2 advances in edge phase against TS1, outputs a "L" signal (at normal operation).</td><td></td></tr>
<tr><td>4</td><td>TEOP</td><td>Tracking error positive output</td><td>O</td><td>When TS2 delays in edge phase against TS1, outputs a "H" signal (at normal operation).</td><td></td></tr>
<tr><td>5</td><td>TES</td><td>Tracking error polarity indication input</td><td>I</td><td>Control signal input used in kick control for search operation</td><td>Pullup resistor incorporated</td></tr>
<tr><td>7</td><td>$\overline{\text{TTAC}}$</td><td>Track TAC output</td><td>O</td><td>Pin outputs clock pulse which the microprocessor is informed of completion of kick or the count number of tracks.</td><td></td></tr>
<tr><td>8</td><td>PUD</td><td>PU motor control input</td><td>I</td><td>Input which stops the PU motor only when the PU motor compulsory-carry signal is a specific code ... (PUD = "H").</td><td></td></tr>
<tr><td>9</td><td>OPNS</td><td>Open/close output</td><td>O</td><td>Output for disc tray drive motor open-close control signal.
"L" = open, "H" = close, HiZ = OFF</td><td>3-state output</td></tr>
<tr><td>10</td><td>DSG</td><td>Data slice control input</td><td>I</td><td>Input for control signal which stops the sub-control of the data slice circuit.
"H" input = OFF.</td><td>Pullup resistor incorporated</td></tr>
</table>

Table 2-2A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin No.	Symbol	Pin name	IN/OUT	Description	Remarks
11	LDC	Laser diode control output	O	Laser diode ON = "H" output, OFF = "L" output	
12	DCON	Dropout control output	O	Output which indicates the dropout position of the RF signal.	
13	PLAY	Play control output	O	Control signal output which operates the PU motor by the PU tracking servo signal.	
14	FOKG	Focus OK output	O	Outputs the OK signal on instruction from the microprocessor when the laser spot is focused. Focus ON = "H" output.	
15	MSP	Disc motor control output	O	Output for disc motor ON/OFF control signal.	
16	TPCO	TES polarity select input	I	Input for signal which selects the polarity of the TES signal used in the kick process circuit. Open (V_{DD}) or connected to GND.	Pullup resistor incorporated
17	EFMI	EFM signal input	I	Input for binary signal obtained by passing the RF signal regenerated by the PU through a comparator. Its polarity should be positive against the RF signal polarity.	Pullup resistor incorporated
18	TS2	Tracking error generation signal (1) input	I	Input for binary signal obtained from passing the $A_2 + A_4$ signal of 4-division photodetector through zero-cross comparator. (Used in tracking error generation.)	Pullup resistor incorporated
19	TS1	Tracking error generation signal (2) input	I	Input for binary signal obtained from passing the $A_1 + A_3$ signal of 4-division photodetector through zero-cross comparator. (Used in tracking error generation.)	Pullup resistor incorporated
20	$\overline{\text{RFOK}}$	RF signal OK input	I	Input for signal indicating the regeneration of the RF signal by the pickup. It turns OFF the data slice (sub) and output EFMO. (At "H")	Pullup resistor incorporated
21	GND	GND			
22	RFES	RF envelope signal input	I	Input for RF presence/absence signal, this signal is obtained by passing the RF envelope detection signal through comparator. It is used in the kick process and dropout process sections.	Pullup resistor incorporated

Table 2-2A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin No.	Symbol	Pin name	IN/OUT	Description	Remarks
23	RFG	RFES control signal output	O	Output which controls the detection level of signal RFES. "L" only during kick operation.	
24~27	MODE4~MODE1	Mode select signal input	I	Input for servo system control signal generation and kick operation process direction indication. Connected to the microprocessor.	Pullup resistor incorporated
28	DSL1	Data slice control (1) output	O	Output for signal obtained by passing signal EFMI through the internal buffer amp. Has the same polarity as signal EFMI.	
29	DSL2	Data slice control (2) output	O	Output for data slice control sub circuit. Detects the variation in slice level by check of the jitter of signal EFMI to control the slice level at an optimum level.	
30	MODE-0	Mode select signal input	I	Input for servo system control signal generation and kick operation process direction indication. Connected to the microprocessor.	Pullup resistor incorporated
31	TEST	Test	I	Normally, open or connected to V_{DD}.	Pullup resistor incorporated
32	PUFF	PU motor fast-carry signal output	O	"H" output → FWD, "L" output → BWD, HiZ → OFF	3-state output
33	KICF	PU kick pulse output	O	"H" output → FWD, "L" output → BWD, HiZ → Kick OFF	
34	DIN	Dropout data I/O	I/O	Data I/O connected to shift register for dropout control	
35	DOCK	Dropout control clock pulse output	O	Output for clock signal (with 6 times the FGS frequency) connected to shift register for dropout control	
36	FG4	FG signal output	O	Output for clock signal obtained from 30 division of signal DOCK	
37	CK88	88 kHz clock pulse input	I	Input for approx. 88 kHz reference clock signal	Pullup resistor incorporated
38	MUT	Muting output	O	Output for muting audio signal.	Pullup resistor incorporated

Table 2-2A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin No.	Symbol	Pin name	IN/OUT	Description	Remarks
39	FGS	FG signal input	I	Input for FG signal with 20 pulse/disc rotation. Should have a duty ratio of approx. 50.	Pullup resistor incorporated
40	PLCK	PLL section clock pulse input	I	Input for reference signal (4.32 MHz) to PLL section for EFM signal reading	Pullup resistor incorporated
41	EFMO	EFM output	O	Inversion output of signal EFMI. With signal $\overline{\text{RFOK}}$ "H", is fixed to "L".	
42	V_{DD}	V_{DD}		+5 V	

Table 2-2A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Each data for mode 0 to 3 is passed through the latch circuit, thereby different control signals are generated in the decoder section.

Control mode truth table A)

MODE						*5 TEP	PLAY	*7 FOKG	LDC	MSP	MUTE	PUFF	OPNS	STATE
0	1	2	3	4										
0	0	0	0	0	0	0	0	0	0	0	0	HiZ	HiZ	1 Tray open state 2 Standby mode after judging right/reverse side of the disc 3 Pause mode (1) *1
1	0	0	0	0	1	0	0	0	1	0	0	HiZ	HiZ	At judgement of disc's loading.
0	1	0	0	0	2	(1)	1	1	1	1	1	HiZ	HiZ	1 REV 2 Cue 3 Play mode (1) × 2
1	1	0	0	0	3	(1)	1	1	1	1	0	HiZ	HiZ	BWD kick, REV, F REV, FWD kick, FWD, F FWD, Judgement of right/reverse side of the disc, TOC read.
0	0	1	0	0	4	0	0	0	1	1	0	HiZ	HiZ	Focus servo ON
1	0	1	0	0	5	0	0	1	1	1	0	HiZ	HiZ	Pause mode (2) *3 Focus tracking servo ON
0	1	1	0	0	6	0	0	1	1	1	0	1	HiZ	FWD search
1	1	1	0	0	7	0	0	1	1	1	0	0	HiZ	BWD search, Stop-BWD mode
0	0	0	1	0	8	0	0	0	1	0	0	HiZ	1	Tray close (laser diode: ON)
1	0	0	1	0	9	(1)	1	1	1	1	0	0	HiZ	PU motor kick before BWD search
0	1	0	1	0	A	(1)	1	1	1	1	1	(1)*6	HiZ	Play mode (2) *4
1	1	0	1	0	B	(1)	1	1	1	1	0	1	HiZ	PU motor kick in FWD search
0	0	1	1	0	C	0	0	0	0	0	0	HiZ	1	Tray close (laser diode: OFF)
1	0	1	1	0	D	0	0	0	0	0	0	0	HiZ	Eject-BWD mode
0	1	1	1	0	E	0	0	0	0	0	0	HiZ	0	Tray open (Open from ON of PU, SLT SW)
1	1	1	1	0	F	0	0	0	0	0	0	0	0	Tray open (Open from OFF of PU, SLT SW)

***1 Pause mode 1** The beginning of the first tune is neglected, and the unit pauses. Then, 10 sec later, pause mode is engaged with LD and MD (disc motor) OFF.

***2 Play mode 1** Normal play mode

***3 Pause mode 2** All pause modes other than pause mode 1

***4 Play mode 2** Mode in which FWD pulse is output periodically in play mode 1

***5 TEP** Mode which is engaged only a Latch-SP = 1 (section 5-1). In this case, a "1" output is emitted.

***6 PUFF** With code A, OUT (1) emits a "1" output only at PUD = 0.

***7 FOKG** During continuous kick operation in kick mode, a "0" output is emitted in any mode.

Table 2-2B TC15G008AP Normal mode table

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Search control used in music scan, etc. is performed by the kick control circuit.

Mode 4 0→1

MODE					Stator
0	1	2	3	(X)	
0	0	0	0	0	Kick Reset
1	0	0	0	1	Kick Reset
0	1	0	0	2	BWD1 TRACK KICK
1	1	0	0	3	FWD1 TRACK KICK
0	0	1	0	4	BWD3 TRACK KICK
1	0	1	0	5	FWD3 TRACK KICK
0	1	1	0	6	BWD5 TRACK KICK
1	1	1	0	7	FWD5 TRACK KICK
0	0	0	1	8	BWD7 TRACK KICK
1	0	0	1	9	FWD7 TRACK KICK
0	1	0	1	A	BWD15 TRACK KICK
1	1	0	1	B	FWD15 TRACK KICK
0	0	1	1	C	BWD31 TRACK KICK
1	0	1	1	D	FWD31 TRACK KICK
0	1	1	1	E	BWD CONTINUOUS Kick
1	1	0	0	F	FWD CONTINUOUS Kick

Table 2-2C TC15G008AP Kick mode table

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-3 Process board (X32-1010-00)

2-3-1 IC15 (TMP4740N-5909, 5914) Main microprocessor

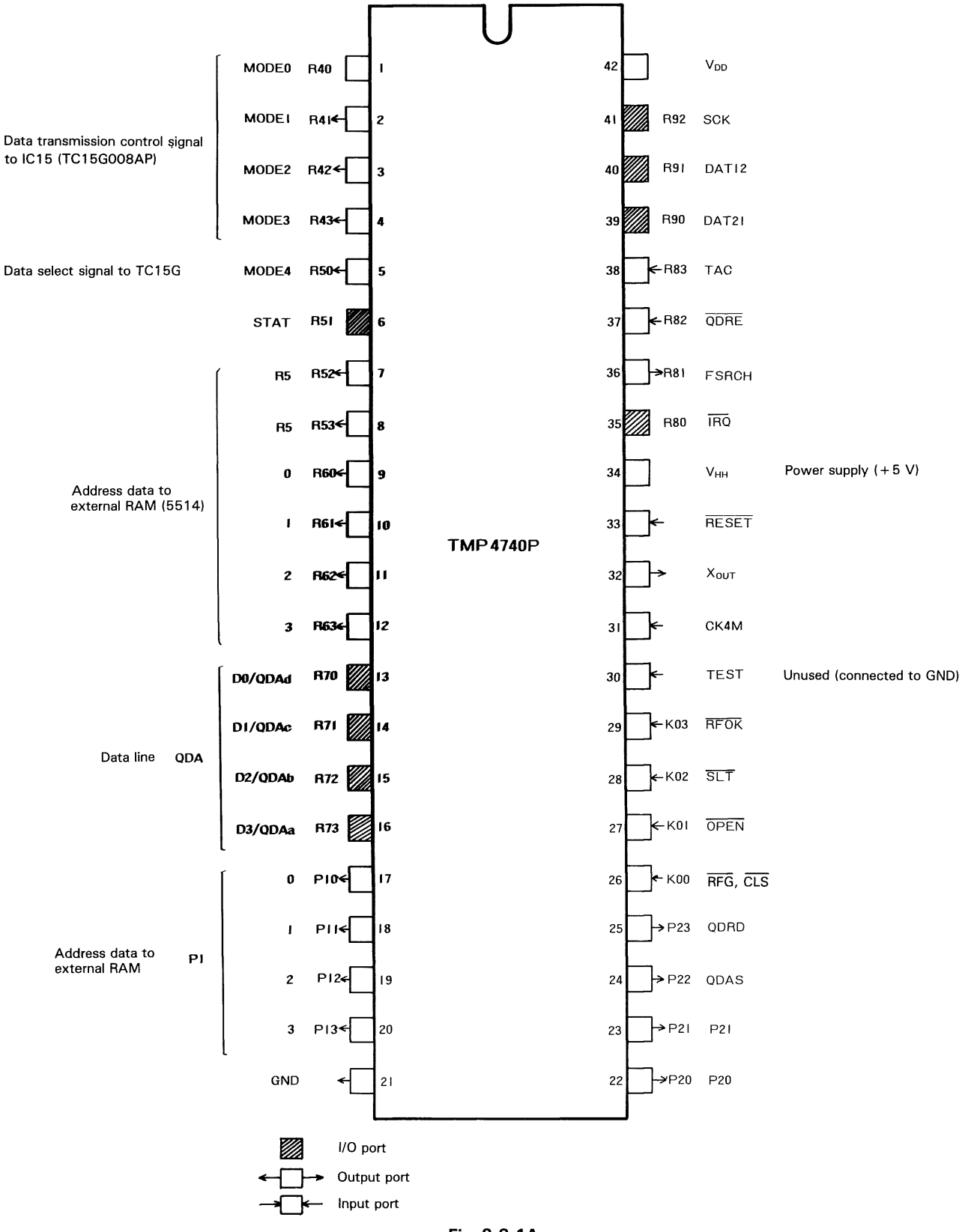


Fig. 2-3-1A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin description of IC15 (TMP4740N)

Pin No.	Port name		Signal name	IN/OUT	Level	Function/operation
1	R4	R40	MD0	O	L	Outputs various mode data and kick data outputs to IC15 (TC15G008AP) for interface with the servo system.
2		R41	MD1	O	L	Outputs various mode data and kick data outputs to IC15 (TC15G008AP) for interface with the servo system.
3		R42	MD2	O	L	Outputs various mode data and kick data outputs to IC15 (TC15G008AP) for interface with the servo system.
4		R43	MD3	O	L	Outputs various mode data and kick data outputs to IC15 (TC15G008AP) for interface with the servo system.
5	R5	R50	MD4	O	L	Data select signal output to IC15 (TC15G008AP). (The kick control data at "H" level and the mode control data at "L" level.)
6		R51	SVCS	I/N	L	Operation start/stop control signal to the servo control microprocessor IC12 (MB88201)
7		R52	A2	O	L	Address data output to the external RAM IC14 (TC-5514P).
8		R53	A1	O	L	Address data output to the external RAM IC14 (TC-5514P).
9	R6	R60	A0	O	H	Address data output to the external RAM IC14 (TC-5514P).
10		R61	A3	O	H	Address data output to the external RAM IC14 (TC-5514P).
11		R62	A4	O	H	Address data output to the external RAM IC14 (TC-5514P).
12		R63	A5	O	H	Address data output to the external RAM IC14 (TC-5514P)
13	R7	R70	DO/QDAd	I/O	H	1 Data input terminal of the subcode Q from IC8 (TC-9178), (T-6391). 2 Data input/output terminal with the external RAM IC14 (TC5514).
14		R71	D1/QDAC	I/O	H	1 Data input terminal of the subcode Q from IC8 (TC-9178), (T-6391). 2 Data input/output terminal with the external RAM IC14 (TC5514).
15		R72	D2/QDAb	I/O	H	1 Data input terminal of the subcode Q from IC8 (TC-9178), (T-6391). 2 Data input/output terminal with the external RAM IC14 (TC5514).
16		R73	D3/QDAa	I/O	H	1 Data input terminal of the subcode Q from IC8 (TC-9178), (T-6391). 2 Data input/output terminal with the external RAM IC14 (TC5514).
17	P1	P10	A6	O	H	Address data to the external RAM IC14 (TC5514).
18		P11	A7	O	H	Address data to the external RAM IC14 (TC5514).
19		P12	A8	O	H	Address data to the external RAM IC14 (TC5514).
20		P13	A9	O	H	Address data to the external RAM IC14 (TC5514).

Table 2-3-1A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin No.	Port name		Signal name	IN/OUT	Level	Function/operation
22	P2	P20	R/W	O	H	Read/write control signal to the external RAM IC14 (TC5514). (''H'' level in read mode and ''L'' level in write mode)
23		P21	QDSE	O	H	Data input select signal to R7 port. (Data from the external RAM IC14 (TC5514) at ''H'' level and the data input of the subcode Q from IC8 (TC-9178) at ''L'' level)
24		P22	QDAS	O	L	CRC error check data and subcode Q data select signal. (Error data at ''L'' level and Q-data at ''H'' level)
25		P23	QDARD	O	L	A signal to read the subcode Q data from IC8 (TC-9178) in 4-bit units. (Data is updated at ''H'' level. One cycle ends every 19 times.)
26	K0	K00	CLS/RFG	I	*	1 Tray close signal input (''L'' level with the tray closed) 2 Kick operation mode signal (''L'' level during the kick operation, and goes to ''H'' level after the kick operation ends.)
27		K01	$\overline{OPN}/\overline{DOK}$	I	*	1 Tray open signal (''L'' level with the tray opened) 2 Disc existence judge signal (''L'' level when a disc exists.)
28		K02	SLT	I	*	Pickup position detect signal input (''H'' level when the pickup is positioned in the program area and ''L'' level in the read-in area.)
29		K03	RFOK	I	*	RF signal input (''L'' level when RF signal exists.)
35	R8	R80	IRQ	I/O	H	Data transfer request signal from IC1 (TMP47C41N) Usually ''H'' level and goes to ''L'' level when the request exists.
36		R81	FSRH	O	L	Focus search signal (≒2 Hz) Usually ''L'' level.
37		R82	QDRE	I	H	A signal to enable reading the subcode Q data from IC8 (TC-9178).
38		R83	TTAC	I	H	Kick end signal
39	R9	R90	DAT21	I/O	L	1 Serial data input from IC1 (TMP47C41N) 2 A signal for controlling data transfer mode with IC1 (TMP47C41N). (''H'' level in transmission mode from IC15 (TMP4740N) to IC1 (TMP47C41N))
40		R91	DAT12	I/O	H	Serial data output to IC1 (TMP47C41N).
41		R92	SCK	I/O	H	Serial data transfer synchronizing signal
21	—		V_{SS}	Power supply	—	Power supply (0 V)
30			TEST	I		Not used (Connected to V_{SS})
31			X_{IN}	I		Oscillator connection terminal
32			X_{OUT}	O		Oscillator connection terminal
33			RESET	I		Initialize signal input

Table 2-3-1A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin No.	Port name		Signal name	IN/OUT	Level	Function/operation
34	—	—	V_{HH}	Power supply	—	Power supply (+5 V)
42		—	V_{DD}	Power supply		Power supply (+5 V)

Table 2-3-1A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-3-2 IC9 (TD6315P) PLL IC

IC9 (TD6315P), the PLL IC developed for CD system DAD player, consists of a digital phase comparator, a charge pump circuit, an active LPF and a data separation circuit.

The digital phase comparator detects the phase error between the clock pulse obtained from 4-division of the VCO output and the reference of the HF signal (EFMI) emitted from the data slicer. Then, from the charge pump circuit, up and down signals UO and DO are output as phase error data.

Pin connection diagram

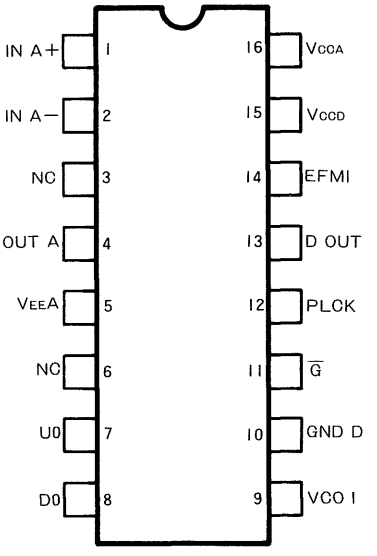


Fig. 2-3-2A

Block diagram

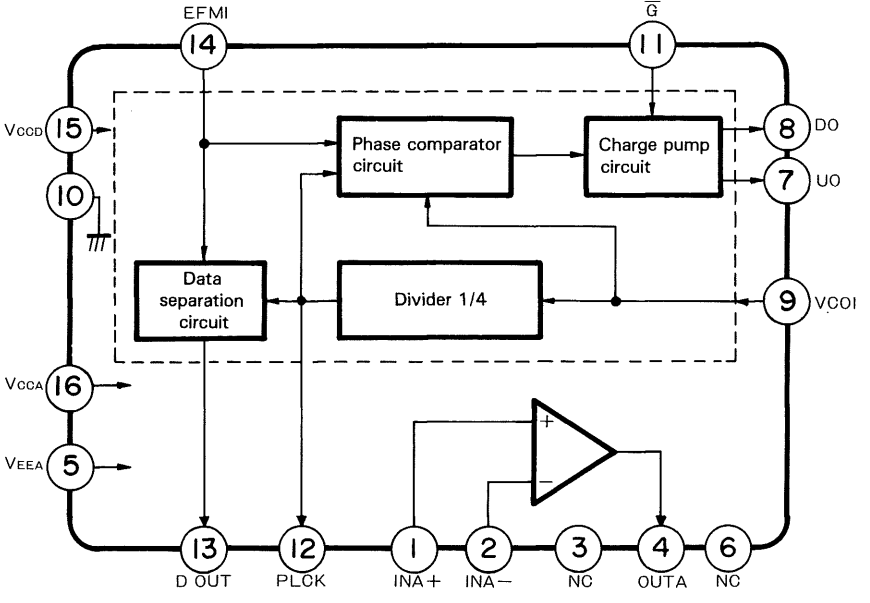


Fig. 2-3-2B TD6315P Block diagram

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin functions

Pin No.	Symbol	Description	Remarks
1	INA+	Positive input of built-in OP amp. Forms the guard ring of INA− together with pin 3 (NC) fixed to approx. 1/2 V_{CCD} voltage.	
2	INA−	Negative input of built-in OP amp. The signal subject to resistance addition by charge pump circuit outputs UO and DO and TC9178F pin TMO is input.	
3	NC	Not used. This pin connected to pin INA+for giving isolation between pins INA− and OUTA.	
4	OUTA	Output of built-in OP amp. Connected to pin INA− through capacitor C and resistor R, forms a lag lead type filter to control VCO.	
5	V_{EEA}	Negative voltage supply to analog circuit.	
6	NC	Not used. Connected to pin INA+for giving isolation between pin V_{EEA} and each of output pins UO and DO.	
7	UO	Charge pump up signal output pin. When signal PLCK obtained from 4-division of VCO frequency is phase delayed in rising edge against signal EFMI input, its "L" output duration is prolonged to make VCO frequency higher. In phase lock, "L" level = 1/2 PLCK.	High impedance state except during "L" direction.
8	DO	Charge pump down signal output pin. When signal PLCK obtained from 4-division of VCO frequency is phase advanced in rising edge against signal EFMI input, its "H" output duration is prolonged to make VCO frequency lower. In phase save, "H" level = 1/2 PLCK.	High impedance state except during "H" period
9	VCOI	Input pin of VCO output signal. The signal subject to AC coupling by a capacitor is input.	
10	GND	GND pin for digital circuit	
11	G	Input by which charge pump outputs UO and DO are made into high impedance. When made "L", high impedance mode is entered to hold the VCO frequency.	TTL level
12	PLCK	Output of data separation clock pulse generated from EFMI input signal in PLL circuit. This output, obtained from 4-division of VCO frequency (17.3 MHz), is input to PLCK of C-MOS processor TC9178F. The clock pulse is 4.32 MHz with duty ratio of 50.	C-MOS leve

Table 2-3-2A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin No.	Symbol	Description	Remarks
13	DOUT	Signal EFMI output. This output, synchronized with the rising edge of signal PLCK, is input to pin EFMI of C-MOS processor TC9178F.	C-MOS level
14	EFMI	Input for EFMI signal obtained by passing the RF signal regenerated from disc through data slicer.	TTL level
15	V_{CCD}	Voltage supply to digital circuit.	
16	V_{CCA}	Positive voltage supply pin to analog circuit.	

Table 2-3-2A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-3-3 IC8 (TC9178F) E.F.M decoder Pin Description

Pin connection

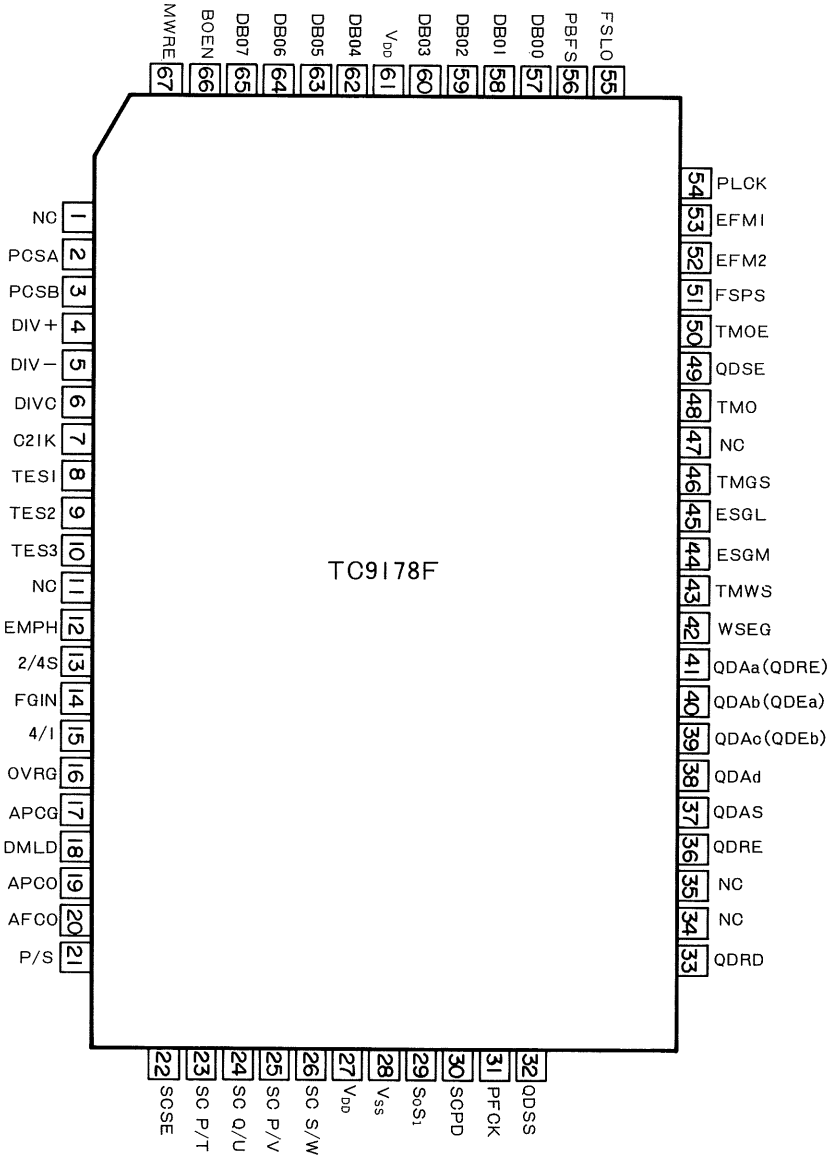


Fig. 2-3-3A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

TC9178F Block diagram

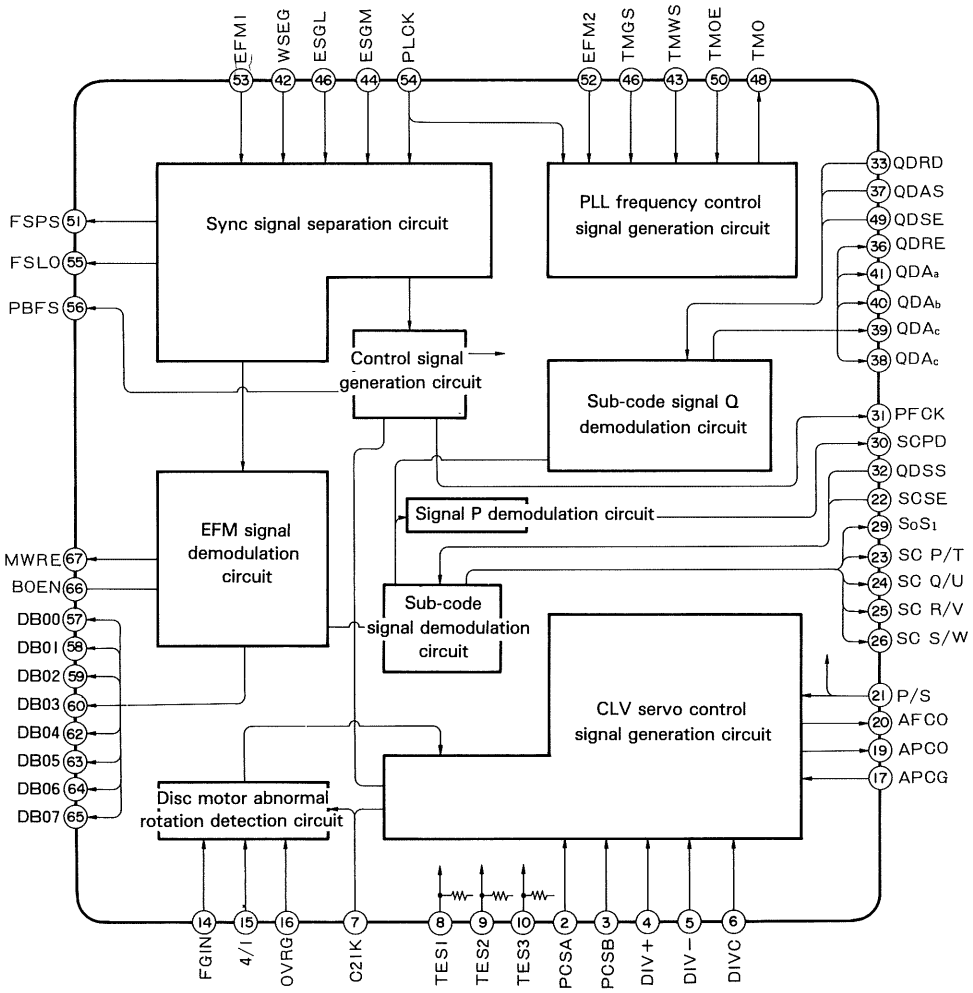


Fig. 2-3-3B

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin functions

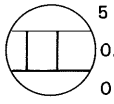
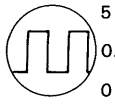
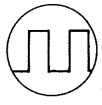
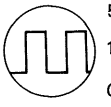
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>1</td><td>NC</td><td>—</td><td>—</td><td>Not connected</td><td></td></tr>
<tr><td>2
3</td><td>PCSA
PCSB</td><td>I</td><td></td><td>These inputs determines the phase comparison frequency.
Phase comparison frequency = 7.35 kHz (frame sync signal)/N
<table>
<tr><th>PCSA</th><th>PCSB</th><th>N</th><th>fc (Hz)</th></tr>
<tr><td>L</td><td>L</td><td>6</td><td>1225</td></tr>
<tr><td>H</td><td>L</td><td>8</td><td>918.75</td></tr>
<tr><td>L</td><td>H</td><td>17</td><td>612.5</td></tr>
<tr><td>H</td><td>H</td><td>16</td><td>459.375</td></tr>
</table></td><td></td></tr>
<tr><td>4</td><td>DIV+</td><td>I</td><td> 
5 V
0.5 μS
0 V
(Appears only at low disc rotation.)</td><td rowspan="3">Input for setting reference frequency division coefficient in APC signal generation circuit for CLV servo control.
Input as buffer memory status signal from TC9179F (IC6).
In addition, the varying amount is selectable by DIVC.
<table>
<tr><th>DIV+</th><th>DIV−</th><th>DIVC</th><th>Reference frequency division coefficient</th><th>Disc motor speed</th></tr>
<tr><td>L</td><td>L</td><td>*</td><td>1/288</td><td></td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>1/287.5</td><td>Higher</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>1/287</td><td>Higher</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>1/288.5</td><td>Lower</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>1/289</td><td>Lower</td></tr>
<tr><td>H</td><td>H</td><td>*</td><td>1/288</td><td></td></tr>
</table>
* Don't care</td><td rowspan="3">Connected to each of TC9179F DIV+ (pin 65) and DIV− (pin 64)</td></tr>
<tr><td>5</td><td>DIV−</td><td>I</td><td> 
5 V
0.5 μS
0 V
(Appears only at high disc rotation.)</td></tr>
<tr><td>6</td><td>DIVC</td><td>I</td><td></td></tr>
<tr><td>7</td><td>C21K</td><td>I</td><td> 
5 V
0.2 μS
0 V</td><td>2.1168 MHz input. This signal, the clock pulse obtained from 4-division of X'tal OSC frequency 8.4672 MHz, is input from TC9179F (IC6). Its duty ratio is 50.</td><td>Connected to CK2M (pin 56) of TC9179F (IC6)</td></tr>
<tr><td>8 ~ 10</td><td>TES-1 ~
TES-3</td><td>I</td><td></td><td>Test inputs, which operates normally at "H" or open state.</td><td>Pullup resistor incorporated</td></tr>
<tr><td>11</td><td>NC</td><td>—</td><td></td><td>Not connected.</td><td></td></tr>
<tr><td>12</td><td>EMPH</td><td>O</td><td></td><td>Output for emphasis presence/absence judgement represented by control bit of sub-code signal Q.
"H" = de-emphasis ON</td><td></td></tr>
</table>

Table 2-3-3A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>13</td><td>2/4S</td><td>O</td><td>—</td><td>Output for CH 2/CH 4 selection judgement represented by control bit of sub-code signal Q.
"L" = CH 2, "H" = CH 4</td><td></td></tr>
<tr><td>14</td><td>FG IN</td><td>I</td><td> 

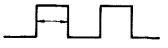
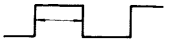
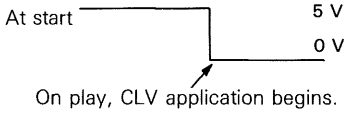
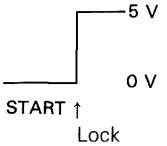
(4 pulses/disc rotation)
Near disc center
 
Near disc edge
  </td><td>Input for FG pulse from disc motor.
1 or 4 pulse per each rotation of disc motor is fed to control speed of the motor within the range of 170 to 400 rpm.
<table>
<tr><th>Disc motor speed (rpm)</th><th>AFCO</th><th>APCO</th></tr>
<tr><td>-175</td><td>Fixed to "H"</td><td>Fixed to 50% duty cycle output</td></tr>
<tr><td>175-740</td><td>Normal operation</td><td>Normal operation</td></tr>
<tr><td>740-</td><td>Fixed to "L"</td><td>Fixed to 50% duty cycle output</td></tr>
</table></td><td></td></tr>
<tr><td>15</td><td>4/1</td><td>I</td><td></td><td>FG IN pulse setting. Either of 1 or 4 pulse per each rotation can be set.
<table>
<tr><th>4/1</th><th>FG pulse per each disc motor rotation</th></tr>
<tr><td>"H" level</td><td>1</td></tr>
<tr><td>"L" level</td><td>4</td></tr>
</table></td><td></td></tr>
<tr><td>16</td><td>OVRG</td><td>I</td><td> 
</td><td>Pin to select whether or not disc motor rotation control is performed by FG IN input.
"H" - FG IN input valid</td><td></td></tr>
<tr><td>17</td><td>APCG</td><td>I</td><td>"H"</td><td>ON/OFF selection input of APC signal generator for CLV servo control.
"L" (generator OFF): APC output is fixed to phase difference "0" that is duty ratio of 50. At the same time, as the internal phase comparison reference frequency generation section is arranged into phase difference "0" against the controlled frequency, the start point of phase comparison when the generator is changed from OFF to ON is set to phase difference "0".</td><td></td></tr>
<tr><td>18</td><td>DMLD</td><td>O</td><td> 
</td><td>Disc motor lock detection output of AFC signal generator for CLV servo control.
Detects the frequency of the frame sync signal. When the frequency is within ±5% deviation, it is set. When the frequency is over ±10 deviation, it is reset. This output signal is the flip-flop output signal. When set, this flip-flop output becomes "H". This output, connected to pin APCG, is used for control of APC block.</td><td></td></tr>
</table>

Table 2-3-3A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

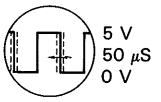
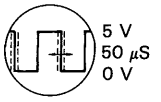
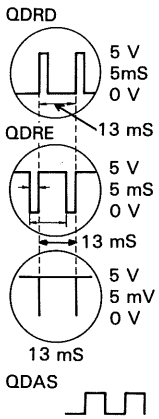
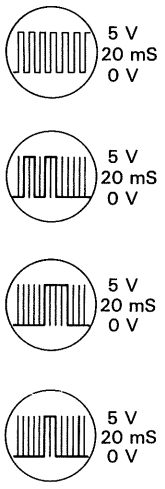
Pin No.	Symbol	I/O	Waveform	Description	Remarks
19	APCO	O		APC signal output for CLV servo control. The output is a PWM (Pulse Width Modulation) wave with resolution = 8 bits, carrier frequency = 8.27 kHz and linear output range = 8 π/9.	
20	AFCO	O		AFC signal output for CLV servo control. The output is a PWM wave with resolution = 8 bits, carrier frequency = 8.27 kHz and linear output range = ±10%.	
21	P/S	I	"H"	CLV servo control signal ON/OFF input. At play, this pin is set to "H" and, at stop, to "L". This input signal is given the highest priority in the CLV servo control system. When this pin is "L", AFC output is fixed to "L", and APC output gets duty ratio of 50.	—
22	SCSE	I	—	Data selection input for 4 outputs of sub-code signal SCT/T - S/W "L" level: Data of 4 bits, P, Q, R and S is output. "H" level: Data of 4 bits T, U, V and W is output.	
23-26	SC P/T SC Q/U SC R/V SC S/W	O	—	8-bit data output of sub-code signal P, Q, R, S, T, U, V, W. This signal is the data of each frame. Here, 4-bit data is output by signal SCSE as required. Data selection of each frame is performed in synchronization with the rising edge of signal PFCK.	Not connected
27	V_{DD}	—	—	Voltage supply pin.	
28	V_{SS}	—	—	GND pin	
29	S_0S_1	O	—	When sub-code signal pattern SO or S1 is detected, this output becomes "H" for that input frame period.	Not connected
30	SCPD	O	—	Output to indicate the date contents of sub-code signal P. Data obtained when the data of each frame is checked in units of 5 frames by the sub-code signal P detection section is output.	Not connected
31	PFCK	O	—	The frame period output with duty ratio of 50. The sub-code data is switched in synchronization with the falling edge of this output.	Not connected

Table 2-3-3A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>32</td><td>QDSS</td><td>I</td><td>"H"</td><td>Input for sub-code sync pattern detection mode selection, demodulating sub-code signal Q.</td><td></td></tr>
<tr><td>33</td><td>QDRD</td><td>I</td><td rowspan="3"> 

With block error</td><td>Input used in reading the sub-code signal Q data inside internal memory in units of 4 bits via outputs QDA-a to QDA-d. When signal QDRD becomes "H", the next 4-bit data is set to pins QDA-a to QDA-d after an arbitrary period from that pulse edge.</td><td></td></tr>
<tr><td>36</td><td>QDRE</td><td>O</td><td>Enable signal output reading sub-code signal Q. When error judgement of 80-bit input sub-code signal Q data is completed, those 4-bit data of MSB side are set to pin QDA-a to QAD-d, and output QDRE becomes "H".
When 20 pulses are input to QDRD or when data Q in the next block is written before the data written in internal RAM is read out, output QDRE becomes "L" so that data reading is disabled.</td><td></td></tr>
<tr><td>37</td><td>QDAS</td><td>I</td><td>Data selection input for sub-code signal Q data outputs QAD-a to QAD-d. For easier interface with the microprocessor, this input determines output data at QDA-a to b, QDRE and QDE ports.
<table><tr><th>QDAS \ Port</th><th>QDAa</th><th>QDAb</th><th>QDAc</th><th>QDAd</th></tr><tr><td>L</td><td>QDRE</td><td>QDEa</td><td>QDEb</td><td>L</td></tr><tr><td>H</td><td>QDAa</td><td>QDAb</td><td>QDAc</td><td>QDAd</td></tr></table></td><td></td></tr>
<tr><td>34, 35</td><td>NC</td><td>—</td><td>Not connected.</td><td></td><td></td></tr>
<tr><td>38</td><td>QDA-d</td><td rowspan="4">O</td><td rowspan="4"> 

(Example of waveform)</td><td rowspan="4">The 80-bit sub-code signal Q data, the block error judgement result of the sub-code signal Q data output or signal QDRE, is output according to the "L" or "H" setting of QDAS. For data transfer to the microprocessor, QDAS is made "L" first, then the error judgement result of data Q is transferred and signal QDRD is input with QDAS "L". Thus, data Q is transferred in units of 4 bits as required.
In addition, QDA-a to QDA-d are 3-state outputs, where selection between output mode and high-impedance mode is made by "L" or "H" of QDSE.
<table><tr><th>QDEa</th><th>QDEb</th><th>Result of judgement</th><th>Output data processing</th></tr><tr><td>H</td><td>H</td><td>No error</td><td>Direct output</td></tr><tr><td>L</td><td>H</td><td>1-bit error of CRCC</td><td>Direct output</td></tr><tr><td>H</td><td>L</td><td>1-bit error of data Q</td><td>1-bit correction output</td></tr><tr><td>L</td><td>L</td><td>Error of 2 bits or more</td><td>Direct output</td></tr></table></td><td rowspan="4"></td></tr>
<tr><td>39</td><td>QDA-c</td></tr>
<tr><td>40</td><td>QDA-b</td></tr>
<tr><td>41</td><td>QDA-a</td></tr>
</table>

Table 2-3-3A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>42</td><td>WSEG</td><td>I</td><td>—</td><td>Window selection of gate signal which, when the frame sync pattern of EFM signal is detected, determines whether or not this pattern is given as the sync signal for the internal system.
<table><tr><td>WSEG</td><td>Gate signal window (number of clocks PLCK)</td></tr><tr><td>L</td><td>±3</td></tr><tr><td>H</td><td>±7</td></tr></table></td><td></td></tr>
<tr><td>43</td><td>TMWS</td><td>I</td><td>—</td><td>Selects the number of Tmax = N (PLCK) in detection of T_{max} of EFM signal which is input from pin EFM2.
<table><tr><td>TMWS</td><td>N (PLCK)</td></tr><tr><td>L</td><td>11±1</td></tr><tr><td>H</td><td>11±0.5</td></tr></table></td><td></td></tr>
<tr><td>44</td><td>FSGM</td><td rowspan="2">I</td><td rowspan="2">—</td><td rowspan="2">When no frame sync pattern is detected within the window of the frame sync separation protection gate signal in N continuous frames, system synchronization is made by the next input frame sync pattern without the window.
These two inputs are used in selection of number N.
<table><tr><td>FSGL</td><td>FSGM</td><td>N (frame)</td></tr><tr><td>L</td><td>L</td><td>12</td></tr><tr><td>H</td><td>L</td><td>8</td></tr><tr><td>L</td><td>H</td><td>4</td></tr><tr><td>H</td><td>H</td><td>2</td></tr></table></td><td rowspan="2"></td></tr>
<tr><td>45</td><td>FSGL</td></tr>
<tr><td>46</td><td>TMGS</td><td>I</td><td>—</td><td>To prevent faulty Tmax detection, data is valid only when data Tmax continues N times. This number N is determined by the input.
<table><tr><td>TMGS</td><td>N</td></tr><tr><td>L</td><td>7</td></tr><tr><td>H</td><td>4</td></tr></table></td><td></td></tr>
<tr><td>47</td><td>NC</td><td>—</td><td>—</td><td>Not connected.</td><td></td></tr>
</table>

Table 2-3-3A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

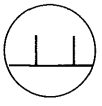
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>48</td><td>TMO</td><td>O</td><td>"DC 2.5 V"
~3.0 V</td><td>The frequency data obtained from Tmax detection of EFM signal which is input from EFM2 is output in one of 3 states as the result of comparison between signal PLCK and Tmax. This output can be used as the frequency status for the PLL circuit.
When P/S signal is "L" (stop mode), output TMO is compulsorily fixed to "H".
<table>
<tr><th>EFM signal frequency status</th><th>TMO</th></tr>
<tr><td>$f_{Tmax} > f_{PLCK}$</td><td>L</td></tr>
<tr><td>$f_{Tmax} \fallingdotseq f_{PLCK}$</td><td>High impedance</td></tr>
<tr><td>$f_{Tmax} > f_{PLCK}$</td><td>H</td></tr>
</table></td><td></td></tr>
<tr><td>49</td><td>QDSE</td><td>I</td><td>"H"</td><td>Input of "H" compulsorily makes outputs QDA-a to QDA-d into high impedance state. This input enables effective use of microprocessor input ports.</td><td></td></tr>
<tr><td>50</td><td>TMOR</td><td>I</td><td rowspan="2">This appears when no synchronization is obtained over some frames.
 
20 mS
5 V
0 V</td><td>Input of "L" compulsorily makes output TMO into high impedance state. Normally, it is connected to FSPS or FSLO.</td><td></td></tr>
<tr><td>51</td><td>FSPS</td><td>O</td><td>Output to indicate the system sync state on the frame sync pattern. Becomes "H" when no sync pattern is given within the window of gate signal in N continuous frames on selection by input FSGL or FSGM.</td><td></td></tr>
<tr><td>52</td><td>EFM2</td><td>I</td><td> 
5 V
0.2 μS
0 V</td><td>Input of EFM signal regenerated from disc. The signal obtained by slicing the signal from the RF amp by the level comparator is directly input (asynchronous to signal PLCK).</td><td></td></tr>
<tr><td>53</td><td>EFM1</td><td>I</td><td> 
4.2 V
0.2 μS
0.4 V
0 V</td><td>Input for EFM signal regenerated from disc. Differently from input signal EFM2, this signal is synchronized to falling edge of signal PLCK phase-locked in the PLL circuit.</td><td></td></tr>
<tr><td>54</td><td>PLCK</td><td>I</td><td> 
4.4 V
0.2 μS
0 V</td><td>Clock pulse input for frame sync separation. This signal is fed from external PLL circuit based on HF signal reproduced from disc. This Clock pulse signal is locked to 4.32 MHz and have duty ratio of 50.</td><td></td></tr>
</table>

Table 2-3-3A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

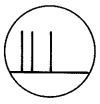
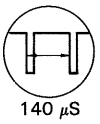
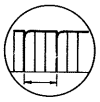
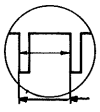
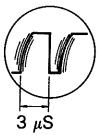
Pin No.	Symbol	I/O	Waveform	Description	Remarks
55	FSLO	O	 5 V 2 mS 0 V	When each system is in synchronization by the frame sync pattern, and when that input pattern is completely synchronized with the frame sync pattern in internal frame counter (the frame synchronization necessarily has 588 pulses PLCK), "L" is output during the frame period.	Not connected
56	PBFS	O	 5 V 50 μS 0 V 140 μS	When "H" is output with a frame sync signal, demodulation data U_0 to U_{31} are transferred to TC9179 (IC6). If "H" which acts as an enable flag, symbol data U_0 to U_{31} transfer will be possible by MWRE.	* Note Connected to PBFS (pin 2) of TC9179F (IC6)
57~60 62~65	DB00-DB07	O	 5 V 0.2 μS 0 V	Outputs for demodulation data U_0 to U_{31} in each frame. These are 3-state outputs. When pin BOEN is "L", data is output. DB00 (LSB) to DB07 (MSB)	* Note Connected to I/O 0 - 7 (pins 19-26) of TC9179F (IC6)
66	BOEN	I	 5 V 1 μS 0 V 3.8 μS	Input for enable signal which turns ON the DB00 to BD07 bus driver.	* Note Connected to BOEN (pin 4) of TC9179F (IC6)
67	MWRE	O	 5 V 1 μS 0 V 3 μS	Output for the enable signal which makes memory write enable. Becomes "L" at the timing at which data is set to the DB00 to DB07 data transfer register. When pin BOEN is "H" and it becomes "L" when pin MWRE becomes "H". After signal PBFS becomes "H", it emits 32 outputs every 17 clock pulses PLCK.	DB00

Table 2-3-3A

*** Note** Data are set to register and MWRE is changed to "L" from "H". This means data are ready to be written into the external RAM. In this condition, BOEN ("L" active) from TC9179F turns bus driver on for 8-bit data DB00 to DB07 transfer.
At the same time of DB00 to DB07 data transfer, PBFS signal is sent to TC9179AF as a frame sync signal. When PBFS is "H", U_0 to U_{31} is output.

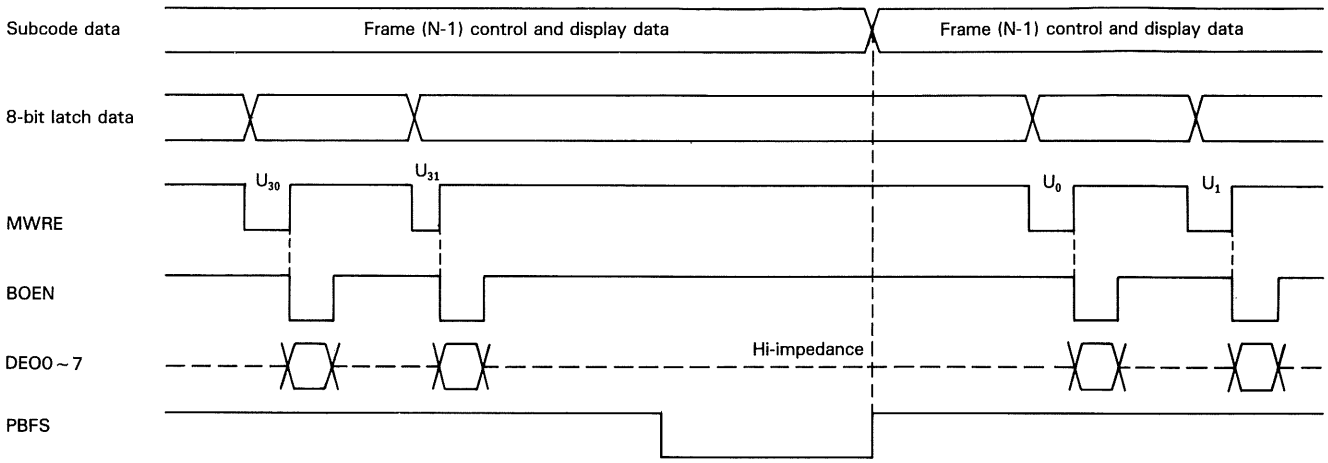


Fig. 2-3-3C EFM demodulation timing diagram

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-3-4 IC6 (TC9179F) Error correction

Pin connection

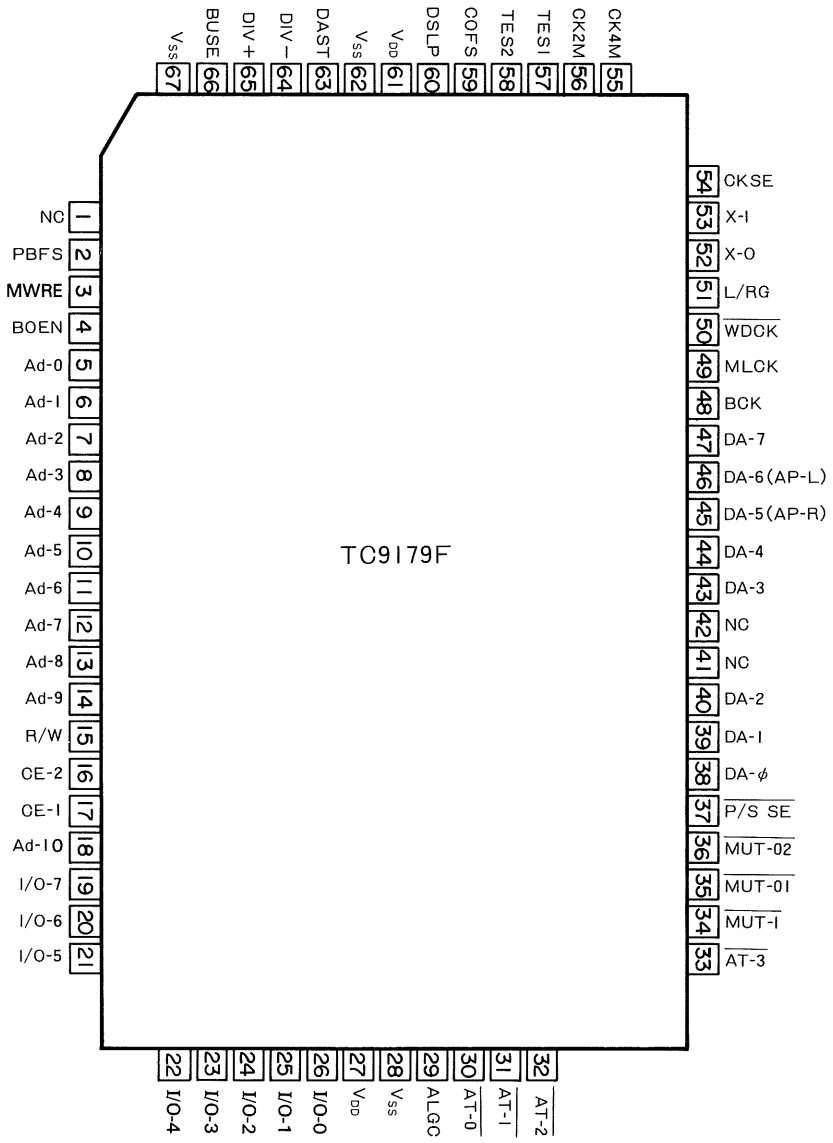


Fig. 2-3-4A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Block diagram

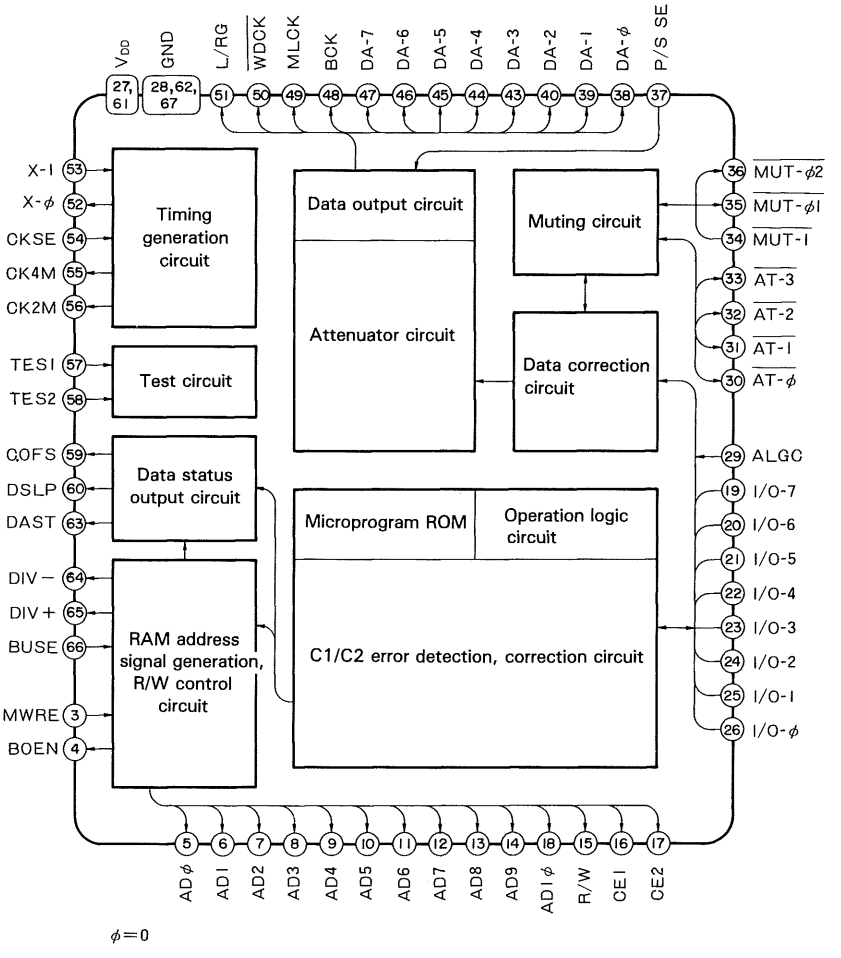


Fig. 2-3-4B TC9179F Block diagram

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin functions

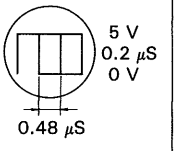
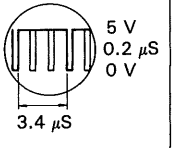
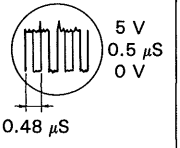
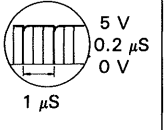
Pin No.	Symbol	I/O	Waveform	Description	Remarks
27, 61	V_{DD}	—	—	Voltage supply pin	
28, 62, 67	V_{SS}	—	—	GND pin	
2	PBFS	I	—	Frame sync input. The symbol data period signal of each frame sent from TC9178F (IC8) is input.	Connected to PBFS (pin 56) of TC9178F (IC8)
3	MWRE	I	—	Memory write request input which accepts MWRE signal from TC9178F (IC8)	Connected to MWRE (pin 67) of TC9178F (IC8)
4	BOEN	O	—	Output enable. When signal MWRE from TC9178F (IC8) can be accepted, the control signal to release symbol data output DB00 to DB07 from Hi-impedance state is output.	Connected to BUSE (pin 66) of TC9178F (IC8)
5~14, 18	AD0~AD9, AD10	O		External RAM address data output. Connected to address data input of external RAM.	
15	R/W	O		Read/write signal output to external RAM. Connected to R/W input of external RAM. "L" = Read, "H" = Write	
16	CE2	O		Chip enable 2 signal is output when external RAM is read or written. Connected to CE2 input of external RAM.	Not connected
17	CE1	O		Chip enable 1 signal is output when external RAM is read or written. Connected to CE1 input of external RAM.	
19~26	I/O-7~ I/O-0	I/O		Data bus line connected to I/O-0 to 7 of external RAM and DB04 -DB07.	

Table 2-3-4A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>29</td><td>ALGC</td><td>I</td><td>—</td><td>Process selection input of C2 correction section. Selects the process algorithm for the frame in which detection of error symbol is not possible in C2 correction section. It is "L" in normal operation.</td><td>Connect to system GND.
(Normal position)</td></tr>
<tr><td>30 ~ 33</td><td>$\overline{\text{AT-0}}$ ~ $\overline{\text{AT-3}}$</td><td>I/O</td><td>—</td><td>Digital attenuator I/O controlled by signal WDCK
WDCK = "L", outputs internal digital attenuator level
WDCK = "H", reads external control data for digital attenuator.
(AT-3 is not connected.)</td><td></td></tr>
<tr><td>34</td><td>$\overline{\text{MUT-1}}$</td><td>I</td><td>—</td><td>Muting control input of the automatic control section of the internal digital attenuator.
At "L", attenuation amount increases (finally, it becomes digital "0"). At "H", attenuation amount decreases (it shifts to 0 dB side).</td><td></td></tr>
<tr><td>35</td><td>$\overline{\text{MUT-01}}$</td><td>O</td><td>—</td><td>Muting 1 output. Outputs an "L" signal when burst error over 64 frames or buffer-over of jitter absorption memory is detected.</td><td></td></tr>
<tr><td>36</td><td>$\overline{\text{MUT-02}}$</td><td>O</td><td>—</td><td>Muting 2 output. Outputs an "L" signal when deinterleave error is detected over 3 continuous frames.</td><td></td></tr>
<tr><td>37</td><td>$\overline{\text{P/S SE}}$</td><td>I</td><td>—</td><td>Output data parallel/serial selection input.
"L" = parallel output, "H" = serial output.</td><td></td></tr>
<tr><td>38</td><td>DA-0</td><td>O</td><td>—</td><td><table><tr><th>$\overline{\text{P/S SE}}$ = "L"</th><th>$\overline{\text{P/S SE}}$ = "H"</th></tr><tr><td>Outputs LSB of 8-bit data.</td><td>Outputs serial data from LSB.</td></tr></table></td><td>Not connected</td></tr>
<tr><td>39</td><td>DA-1</td><td>O</td><td>—</td><td><table><tr><th>P/S SE = "L"</th><th>P/S SE = "H"</th></tr><tr><td>Outputs the second bit from LSB of 8-bit data.</td><td>Outputs correction flag of 8 bits of MSB side.</td></tr></table></td><td>Not connected</td></tr>
<tr><td>40</td><td>DA-2</td><td>O</td><td>—</td><td><table><tr><th>P/S SE = "L"</th><th>P/S SE = "H"</th></tr><tr><td>Outputs the third bit from LSB of 8-bit data.</td><td>Outputs correction flag of 8 bits of LSB side.</td></tr></table></td><td>Not connected</td></tr>
</table>

Table 2-3-4A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

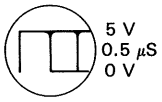
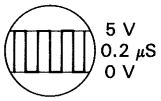
Pin No.	Symbol	I/O	Waveform	Description	Remarks
41, 42	NC	—	—	Not connected.	
43	DA-3	O	—	$\overline{P/S\ SE}$ = "L": Outputs the fourth bit from LSB of 8-bit data. $\overline{P/S\ SE}$ = "H": Outputs a "H" signal when correction flag of LSB side is set side with level of MSB side at −30 dB.	Not connected
44	DA-4	O	—	$\overline{P/S\ SE}$ = "L": Outputs the fifth bit from LSB of 8-bit data. P/S SE = "H": 1 MCK output. Outputs the clock signal (1.058 MHz) obtained from 2-division of signal CK2M.	Not connected
45	DA-5	O	—	$\overline{P/S\ SE}$ = "L": Outputs the sixth bit from LSB of 8-bit data. $\overline{P/S\ SE}$ = "H": APL output. Outputs R-channel aperture signal.	Not connected
46	DA-6	O	—	$\overline{P/S\ SE}$ = "L": Outputs the seventh bit from LSB of 8-bit data. $\overline{P/S\ SE}$ = "H": APL output. Outputs L-channel aperture signal.	Not connected
47	DA-7	O		$\overline{P/S\ SE}$ = "L": Outputs MSB of 8-bit data. $\overline{P/S\ SE}$ = "H": Outputs music data in serial from MSB.	
48	BCK	O		Bit clock pulse is output when serial data is output. Thus, serial data is output in synchronization with the rising edge of this clock pulse (1.4 MHz).	

Table 2-3-4A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

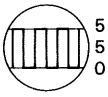
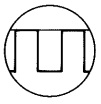
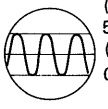
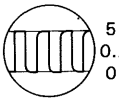
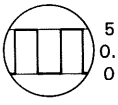
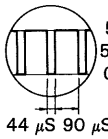
Pin No.	Symbol	I/O	Waveform	Description	Remarks
49	MLCK	O		MSB/LSB clock pulse output. Outputs the clock signal (176.4 kHz) obtained from 8-division of signal BCK, which is used as a set clock pulse when 8-bit parallel data is output.	Not connected
50	WDCK	O	 5 V 5 μS 0 V	Word clock pulse output. Outputs the clock signal (88.2 kHz) obtained from 16-division of signal BCK, which indicates the output period of one word.	
51	L/RG	O	 5 V 5 μS 0 V	Sampling frequency output. Outputs the clock signal (44.1 kHz) obtained from 2-division of signal WDCK, which indicates the data output channel. "L" = L channel, "H" = R channel.	
52	X-0	O	 4.26 V (X−1) 5 V (X−0) 0 V 0.05 μS	X'tal OSC connection pins. X'tal OSC is connected to generate the clock signal required in the system. (Feedback resistance and amp incorporated) X'tal OSC frequency = 8.4672 MHz	
53	X-1	I			
54	CKSE	I	—	Selection pin which informs X'tal OSC frequency. (Pullup resistance incorporated) "H" or open = 8.4672 MHz, "L" = 4.2336 MHz	
55	CK4M	O	 5 V 0.2 μS 0 V	4 MHz clock pulse output. Outputs 4.2336 MHz, which is also used as the clock signal for microprocessor.	
56	CK2M	O	 5 V 0.2 μS 0 V	2 MHz clock pulse output. Outputs 2.1162 MHz, which is used as the clock signal for TC9178F (IC8).	Connected to C21K (pin 7) of TC9178F (IC8)
57	TES1	I		Test pins (pullup resistance incorporated) In normal operation, it is "H" or open.	
58	TES2				
59	COFS	O	 5 V 50 μS 0 V 44 μS 90 μS	Frame period signal output. Outputs corrected frame period signal.	

Table 2-3-4A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

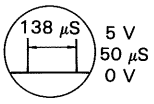
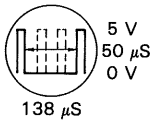
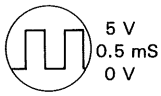
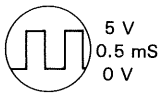
Pin No.	Symbol	I/O	Waveform	Description	Remarks
60	DSLP	O		Data status signal output. (Error information signal output)	
63	DAST	O		Data status signal output. (Error information signal output)	
64	DIV−	O		Buffer memory status output. Outputs an "H" signal when the jitter absorption buffer memory enters range of +2 or +3 frames in its capacity of ±4 frames. This output is connected to pin DIV- of TC9178F (IC8) to lower the disc motor revolution.	Connected to DIV− (pin 5) of TC9178F (IC8)
65	DIV+	O		Buffer memory status output. Outputs an "H" signal when the jitter absorption buffer memory enters range of −2 or −3 frames in its capacity of ±4 frames. This output is connected to pin DIV+ of TC9178F (IC8) to raise the disc motor revolution.	Connected to DIV+ (pin 4) of TC9178F (IC8)
66	BUSE	I		Buffer selection input pin. Selects the output condition of DIV−/DIV+. At "H", Div± output are made when the buffer memory enters range of ±2 frames. At "L", Div± output are made when it enters range of ±3 frames.	

Table 2-3-4A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-3-5 IC12 (MB88201-115K) SVC mircoprocessor

Pin connection diagram

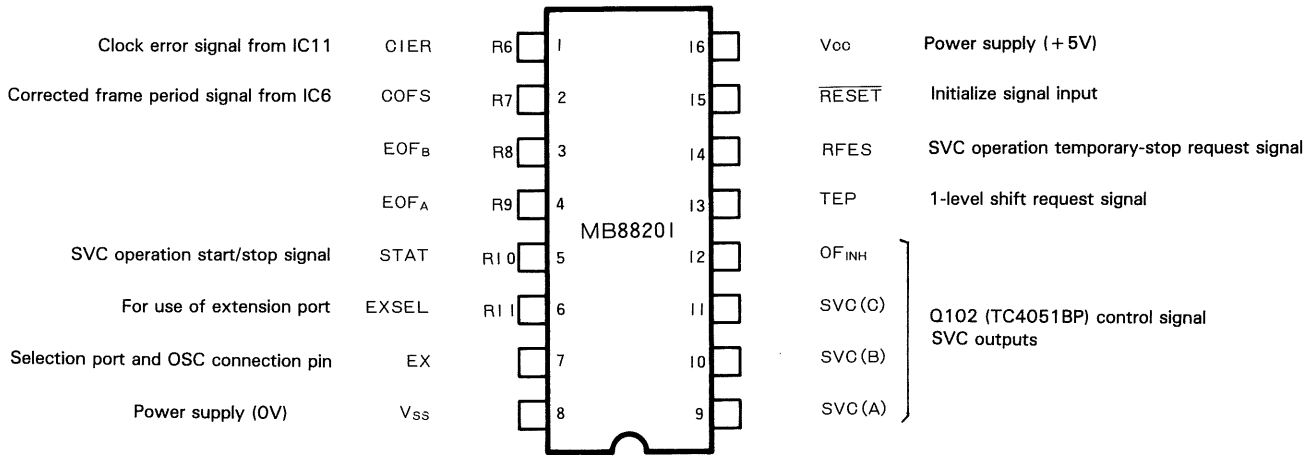


Fig. 2-3-5A

Block diagram

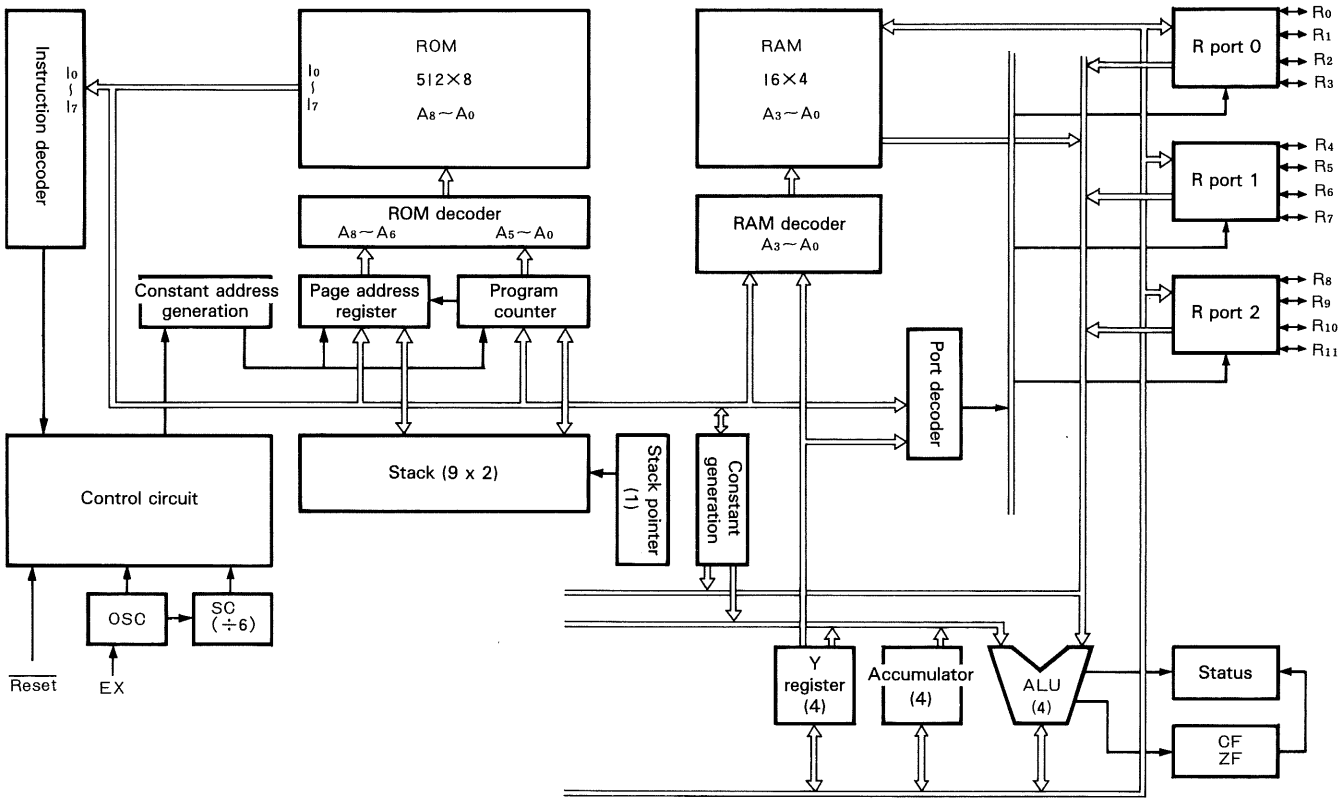


Fig. 2-3-5B

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin functions

Pin No.	Port name	Signal name	I/O	Initial value	Description
9	RO	SVC (A)	O	0	Output for focus offset amount control data to Q102 (SVC circuit) bit 0
10	R1	SVC (B)	O		Output for focus offset amount control data to Q102 (SVC circuit) bit 1
11	R2	SVC (C)	O		Output for focus offset amount control data to Q102 (SVC circuit) bit 2
12	R3	OF_{INH}	O		Output for focus offset amount control data to Q102 (SVC circuit) bit 3
13	R4	TEP	I	1	Input for focus offset amount 1-level shift request signal. During execution of kick operation, becomes "L" to perform 1-level shift.
14	R5	RFES	I	1	Input for SVC operation (counting the number of errors) halts request signal. When track jump occurs, becomes "H". After that, stops operation for 1.2 msec.
1	R6	CIER	I	1	Input for block error signal from IC11. When block error occurs, becomes "H".
2	R7	COFS	I	1	Input for corrected frame period signal (7.35 kHz square wave) from IC6. At the point when it becomes "H" signal CIER is judged.
3	R8	EOF_B	O	1	Output for focus offset amount control data to Q102 (TC4051BP) Not used. bit 1
4	R9	EOF_A	O	1	Not used. Grounded.
5	R10	STAT	I/O	1	SVC operation start/stop control, which is connected to IC15 (TMP4740N). When a "H" signal is input, operation starts, while when a "L" signal is input, operation stops. In addition, when offset amount adjustment is complete, it output a "L" signal with a duration of 3.4 msec.
6	R11	EXSEL	I	1	Not used. Grounded.
7	—	CK2M	I	—	Clock pulse input.
8		V_{SS}			GND pin
15		RESET	I		Initialize signal input.
16		—	Power supply		Power supply (+5 V) pin.

Table 2-3-5A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Operation of IC12 (MB88201)

IC12 (MB88201) is the CPU to control focus offset amount against temperature change, etc. (This control operation is termed SVC operation for short.)

Focus offset amount is controlled by control of bilateral switch Q102 (TC4051BP) through SVC (A) ≅ SVC (C) and OF_{INH}.
The following table shows the relationship between each ports and offset level.

Ports / Level	OF_{INH}	SVC (A)	SVC (B)	SVC (C)	Remarks
2	0	0	1	0	
1	0	1	0	0	
0	0	0	0	0	Initial select offset level
7	0	1	1	1	
6	0	0	1	1	
5	0	1	0	1	
4	0	0	0	1	
3	0	1	1	0	
INH	1	×	×	×	

×: Don't care

Table 2-3-5B

As shown in the table, the offset level can be set to 8 levels. The offset level is determined by the amount of NFB to the focus error amp Q103, i.e. the value of resistor is changed by bilateral switch controlled by SVC (A) to (C), OF_{INH}. The following outlines the focus offset amount adjustment procedure.

Fig. 2-3-5C shows that, starting from the initial offset level, counting of number of block errors executed from level 0. The offset level is stepped down one by one till the count exceeds 2000 (in this case N = A > 2000 at level 3). From the level of which the count exceeded 2000, the offset level is stepped up 3 levels (in this case to level 6: N = B) for enough clearance margin for block error numbers. This level is maintained till the end of playback unless the disc is changed or stopped.

For counting of the number of block errors, the number of times by which block error signal CIER from IC11 (TC4094BP) generated in synchronization with correction frame period signal COFS (7.35 kHz square wave) from IC6 (TC9179F) becomes "H" is counted.

Measurement of the number of block errors at each offset level is done by 256 x 6 samples (rising edges of signal COFS). Normally, this measurement is completed in approx. 0.2 sec. In addition, when signal RFES becomes "H" (when track jump occurs), the measurement is halted for approx. 1.2 msec.

Start and stop of this SVC adjustment operation is controlled by IC15 (TMP4740N). In this case, when STAT becomes "H", this operation starts, while when it becomes "L", the operation stops and focus offset amount returns to the set value before adjustment. Further, when the operation is complete, STAT outputs an "L" signal with a duration of about 3.4 msec to inform IC15 (TMP4740N) of completion.

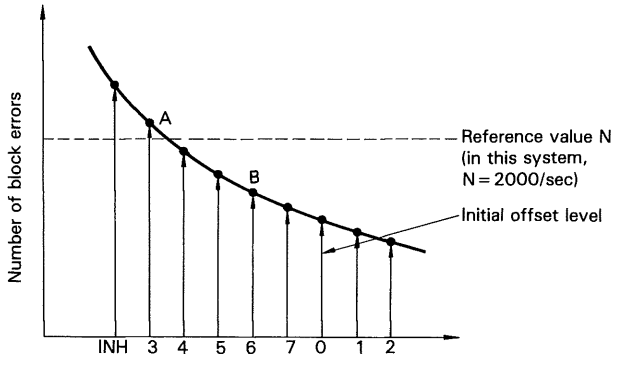


Fig. 2-3-5C

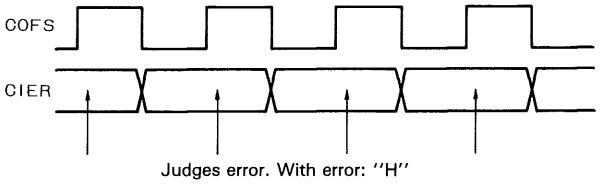


Fig. 2-3-5D

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-3-6 IC14 (TC5514P) T.O.C. Memory

Pin connection diagram

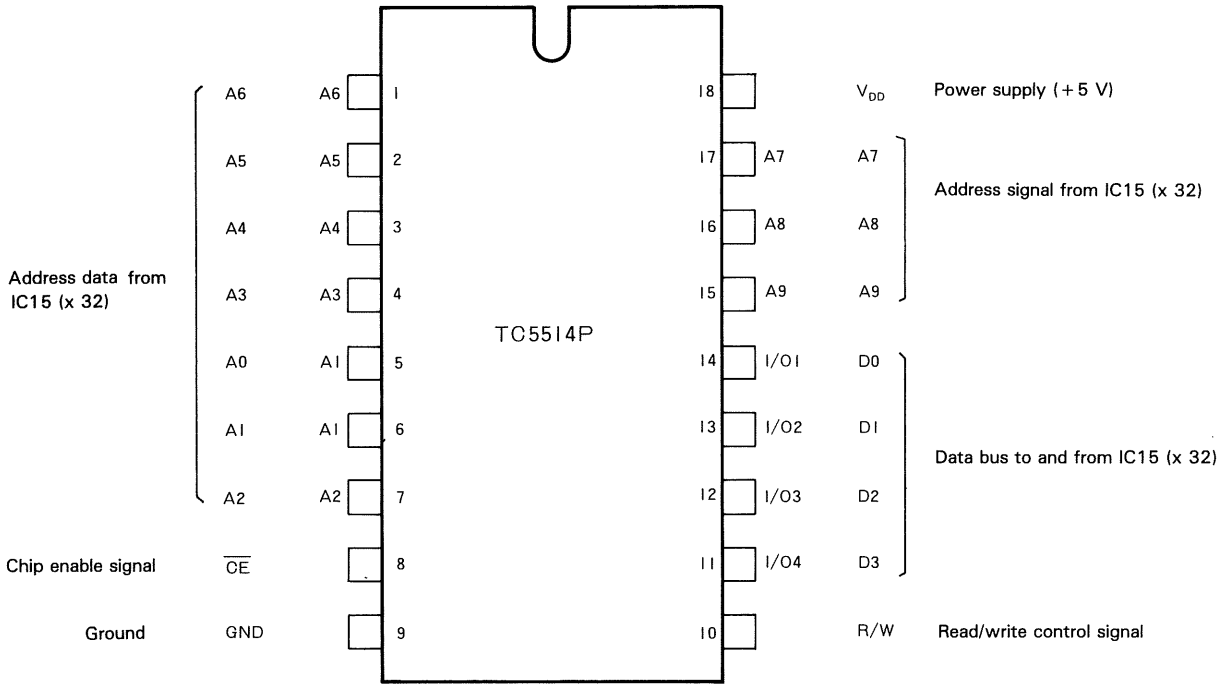


Fig. 2-3-6A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin functions of external RAM IC14 (TC5514P)

Pin No.	Port pin name	Signal name	I/O	Initial value	Description
5	A0	A0	I	*	Address input from IC15 (TC4740N) (X32-1010-11) bit 0
6	A1	A1	I		Address input from IC15 (TC4740N) (X32-1010-11) bit 1
7	A2	A2	I		Address input from IC15 (TC4740N) (X32-1010-11) bit 2
4	A3	A3	I		Address input from IC15 (TC4740N) (X32-1010-11) bit 3
3	A4	A4	I		Address input from IC15 (TC4740N) (X32-1010-11) bit 4
2	A5	A5	I		Address input from IC15 (TC4740N) (X32-1010-11) bit 5
1	A6	A6	I		Address input from IC15 (TC4740N) (X32-1010-11) bit 6
17	A7	A7	I		Address input from IC15 (TC4740N) (X32-1010-11) bit 7
16	A8	A8	I		Address input from IC15 (TC4740N) (X32-1010-11) bit 8
15	A9	A9	I		Address input from IC15 (TC4740N) (X32-1010-11) bit 9
14	I/O1	D0	I		Data in/output from IC15 (TC4740N) (X32-1010-11) bit 0
13	I/O2	D1	I/O		Data in/output from IC15 (TC4740N) (X32-1010-11) bit 1
12	I/O3	D2	I/O		Data in/output from IC15 (TC4740N) (X32-1010-11) bit 2
11	I/O4	D3	I/O		Data in/output from IC15 (TC4740N) (X32-1010-11) bit 3
10		R/W	I		Read/write control signal input. "H" = Read, "L" = Write
8		$\overline{CE}$	I		Chip enable signal input (active "L")
9		GND	Ground		Ground
18		V_{DD}	Power supply		Power supply pin (+5 V)

Table 2-3-6A

Control of external RAM IC14 (TC5514P)

The external RAM is provided with the following data storage areas. Different data are written or read by control of microprocessor ports R6, P1 and R5 (R52, R53) (address designation), port R7 (data I/0), port P2 (P20) (write/read control) or port P2 (P21) (chip enable). (Refer to "Pin functions of IC15", Table 2-3-1A.)

(1) Area of lead-in data (play start time of each tune and read-out start time)
(2) Area of tune No. data (TNO, X) of preset channels (CH 1 - 16)
(3) Area of play time data of each preset channel
(4) Area of total play time of each channel

First, the method of access to the area of read-in data (Area (1)) is described.

As shown in Table 2-3-6A, IC14 is so configured that row address is designated by microprocessor ports R52 and R53, LSB data of column address by 4 ports R6, and MSB data of column address by 4 ports P1. Here, the microprocessor is programmed so that the binary conversion value of the point data (tune No.) which is read, in reading the lead-in data, is set as column address. A compact disc can record up to a maximum of 99 tunes. Thus, area of column addresses H'01 to H'63 (H' before the number or alphabet means that they are expressed in hexadecimal) is used as save area of lead-in data (Area (1)). (read-out start time data is saved in code address H'64.)

In combination with the column address determined in this manner, the 10's digit of minutes data of play start time is saved in address 0 of the row address given by ports R52 and R53, the 1's digit of minutes data is saved in address 1, the 10's digit of seconds data in address 2, and the 1' digit of seconds data in location 3. This operation timing is shown in Fig. 2-3-6B. The remaining three areas (2), (3) and (4) relate with preset channels. For channel presetting, a data save area for 16 channels is needed. To meet this need, the area of column addresses H'80 -H'FF is divided into 16 sections. As shown in Table 2-3-6B, four words of index LSB data, index MSB data, TNO LSB data and TNO MSB data (Area (2)) are saved in row address 0 in order from the head column address of each section, four words of 1's digit of seconds data, 10's digit seconds data, 1's digit of minutes data and 10's digit of minutes data (Area (3)) are in row address 1, and five words of 1's digit of seconds data, 10's digit of seconds digit data, 1's digit of minutes data, 10's digit minutes data and 100's digit of minutes data (Area (4)) are in row address 3. Fig. 2-3-6C shows this operation timing.

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

External RAM IC14 (TC5514P) map RAM capacity, 1023 words Capacity used, 626 words → 4 bit

Column address		R53, R52 (Row address)				Data contents
R1	R6	0	1	2	3	
0	0					
0	1	10 MIN	1 MIN	10 SEC	1 SEC	TNO. 1
0 ⋮ 6	2 ⋮ 1	10 MIN ⋮	1 MIN ⋮	10 SEC ⋮	1 SEC ⋮	TNO. 2 ⋮ TNO. 97
6	2	10 MIN	1 MIN	10 SEC	1 SEC	TNO. 98
6	3	10 MIN	1 MIN	10 SEC	1 SEC	TNO. 99
6	4	10 MIN	1 MIN	10 SEC	1 SEC	Read-out start time
6 ≀ 7	5 ≀ 8	Unused				
7	9	Unused			CH CNTL	Number of memories
7	A				CH CNTH	
8	0	INDEX L	1 SEC	1 SEC	Unused	CH1 CH DATA CH TIME TOTAL TIME
8	1	INDEX H	10 SEC	10 SEC		
8	2	TNO. L	1 MIN	1 MIN		
8	3	TNO. H	10 MIN	10 MIN		
8	4	Unused		100 MIN		
8	5			Unused		
8	6					
8	7					
8	8	INDEX L	1 SEC	1 SEC	Unused	CH 2
8	9	INDEX H	10 SEC	10 SEC		
8	A	TNO. L	1 MIN	1 MIN		
8	B	TNO. H	10 MIN	10 MIN		
8	C	Unused	Unused	100 MIN		
8	D			Unused		
8	E					
8	F					
9	0	The same as in 8-8 to 8-F is repeated.			Unused	CH 3
≀	≀					
F	F					CH 16

<CH DATA> <CH TIME> <TOTAL TIME>

Table 2-3-6B

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

The operation timing when play start time data of 53 min 41 sec is written on the point data of tune 20 which is read out in reading the read-in data.

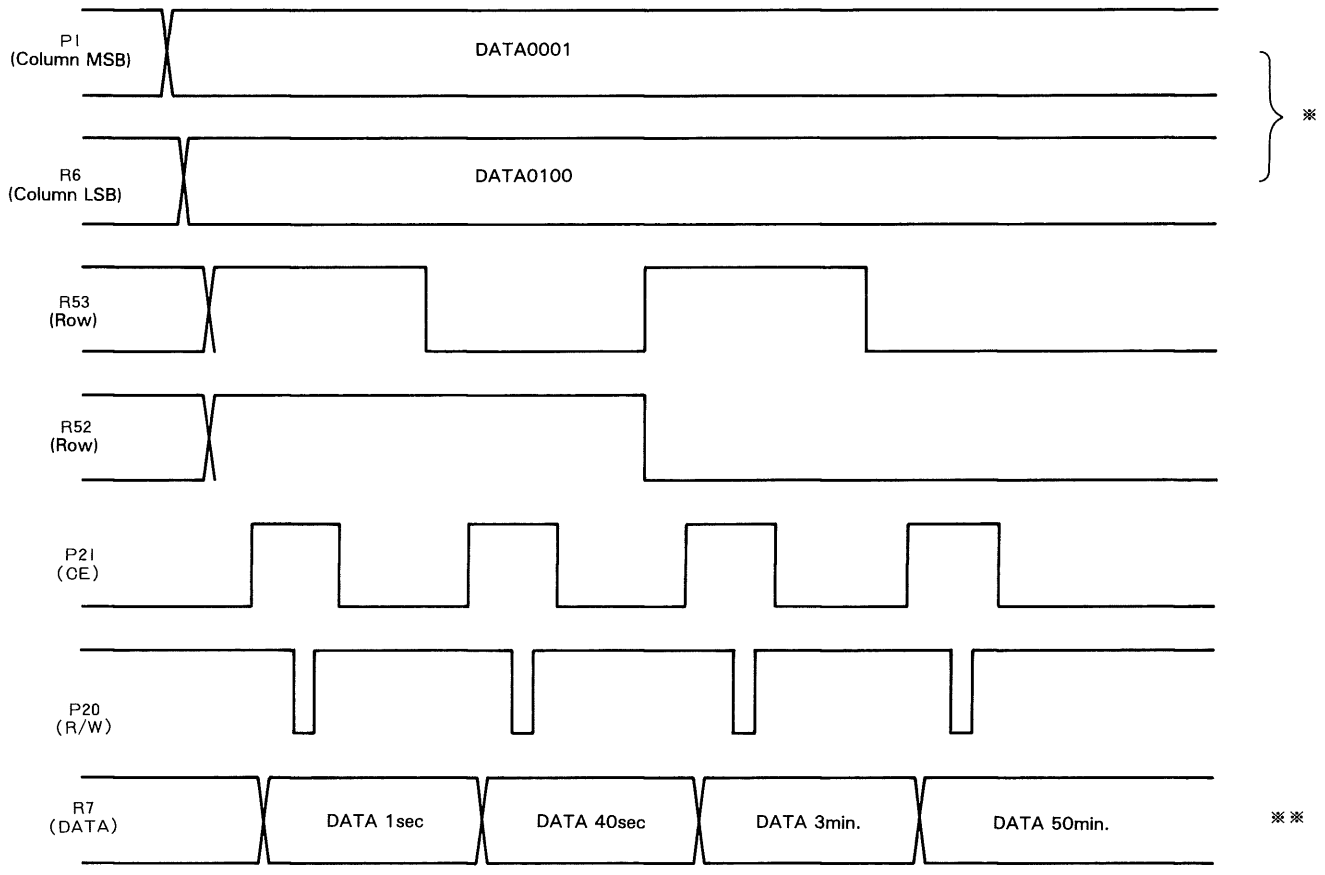


Fig. 2-3-6B

* As mentioned above, the binary conversion data of the point data read out is used as column address. Therefore, in this case (tune 20), the column address is H'14.

** Data is written or read in order from sec digit.

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Operation timing when channel-16 total play time data of 95 min 34 sec is written

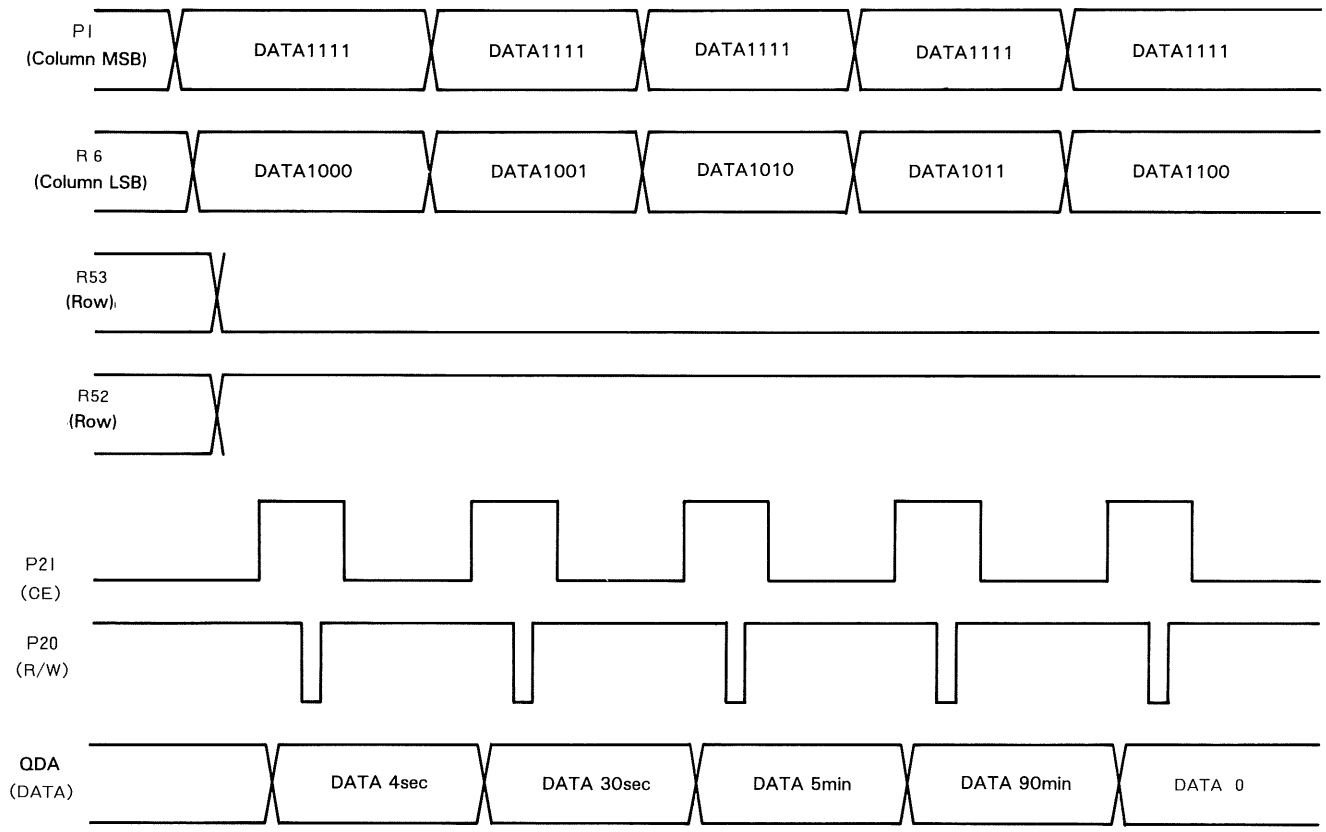


Fig. 2-3-6C

*The head column address for each channel is represented by a hexadecimal number. For this purpose, the result of subtraction by 1 from channel data (CH 1 to CH 16) is converted to a hexadecimal number, to which H'80 is then added. Thus, the result of this addition is used as this head column address. In this case (CH 16), therefore, the head column address is H'F8.

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-3-7 IC26 (μPD4053BC)

Pin connection

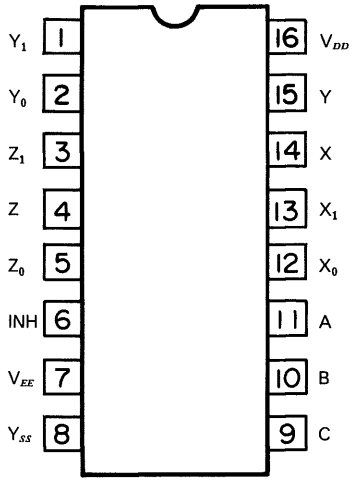


Fig. 2-3-7A

Block diagram

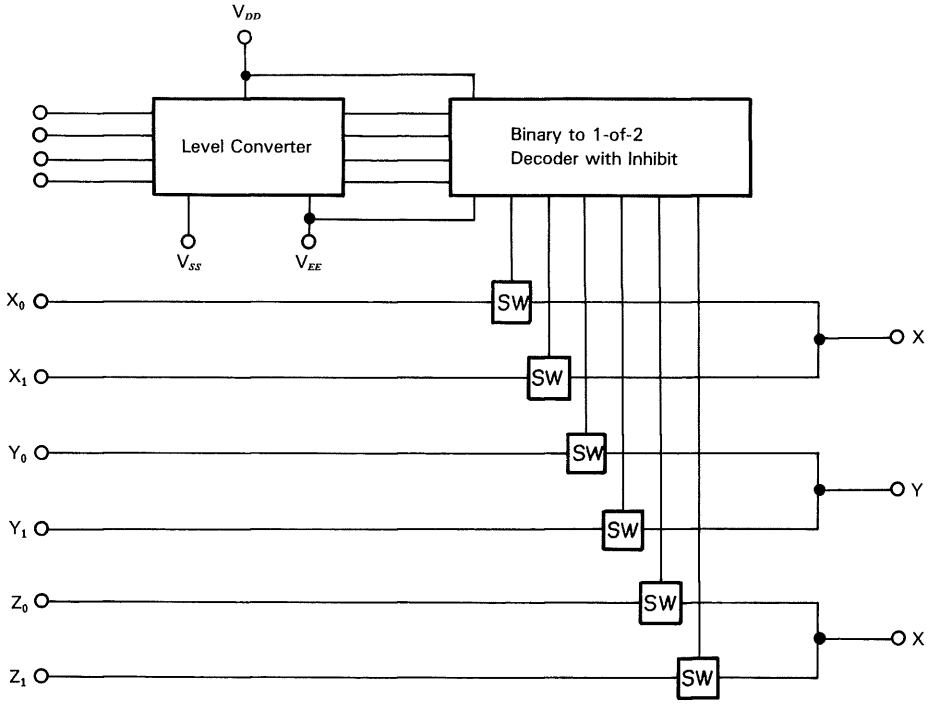


Fig. 2-3-7B

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Turn table

	Control inputs				"ON" Channel
	INHIBIT	C	B	A	
An emphasized→ (Q6 is turned off)	L	L	L	L	Z_0, Y_0, X_0
	L	L	L	H	Z_0, Y_0, X_1
	L	L	H	L	Z_0, Y_1, X_0
	L	L	H	H	Z_0, Y_1, X_1
	L	H	L	L	Z_1, Y_0, X_0
	L	H	L	H	Z_1, Y_0, X_1
	L	H	H	L	Z_1, Y_1, X_0
Not an emphasized→ (Q6 is turned on)	L	H	H	H	Z_1, Y_1, X_1
	H	X	X	X	NONE

"H": High level
"L": Low level
"X": "H" or "L"

Table 2-3-7

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2-4 Display PC board (X25-2020-00)

2-4-1 IC1 (TMP47C41N) display microprocessor

Pin connection diagram

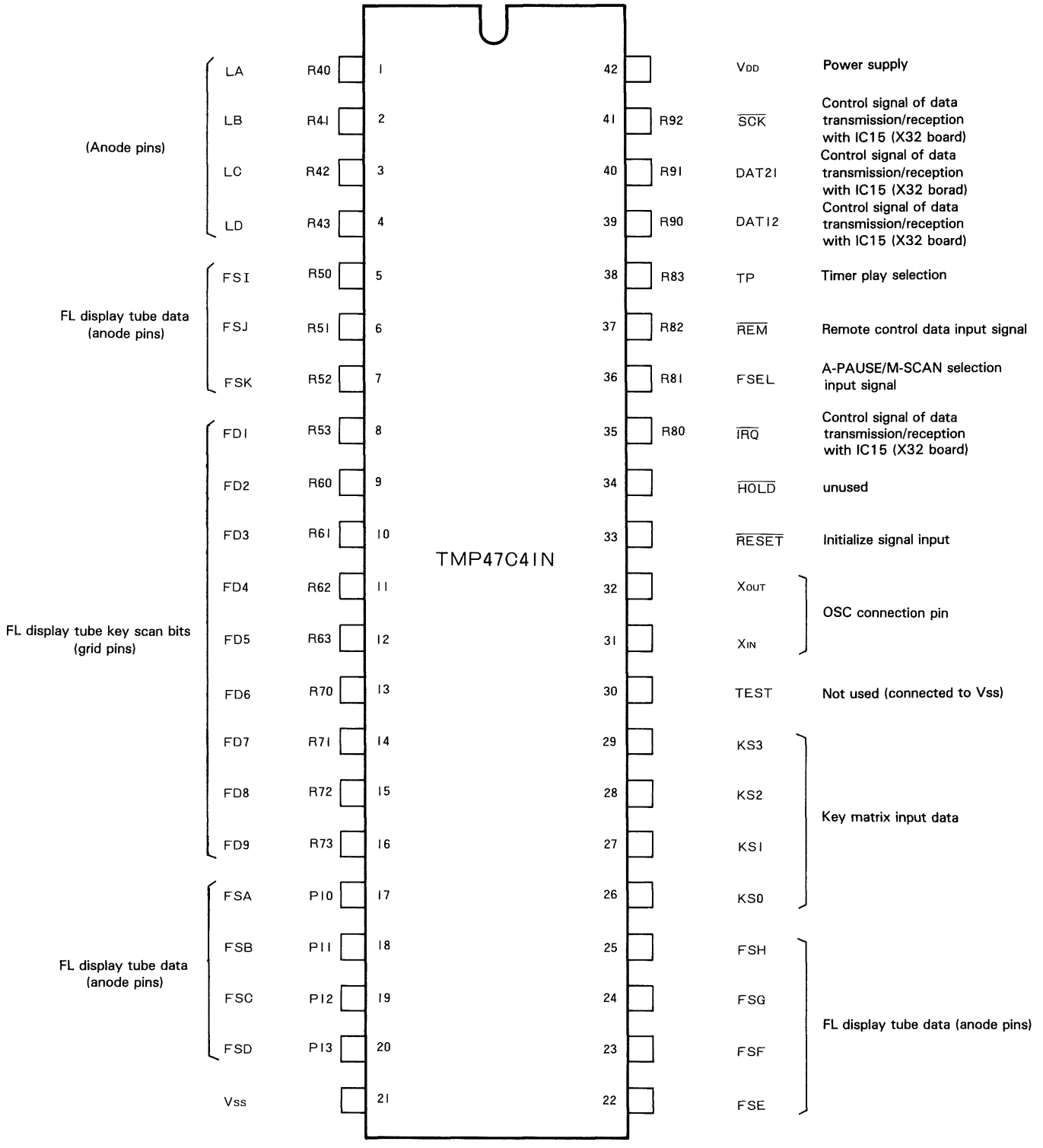


Fig. 2-4-1A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin functions

Pin No.	Port name		Signal name	I/O	Initial value	Description	
1	R4	R40	LA	O	*	(Anode)	Anode A
2		R41	LB	O		(Anode)	Anode B
3		R42	LC	O		(Anode)	Anode C
4		R43	LD	O		(Anode)	Anode D
5	R5	R50	FSI	O	0	FL display tube data (Anode)	Anode I
6		R51	FSJ	O		FL display tube data (Anode)	Anode J
7		R52	FSK	O		FL display tube data (Anode)	Anode K
8		R53	FD1	O		FL display tube data (Grid)	Bit 1
9	R6	R60	FD2	O	0	FL display tube data (Grid)	Bit 2
10		R61	FD3	O		FL display tube data (Grid)	Bit 3
11		R62	FD4	O		FL display tube data (Grid)	Bit 4
12		R63	FD5	O		FL display tube data (Grid)	Bit 5
13	R7	R70	FD6	O	0	FL display tube data (Grid)	Bit 6
14		R71	FD7	O		FL display tube data (Grid)	Bit 7
15		R72	FD8	O		FL display tube data (Grid)	Bit 8
17		R73	FD9	O		FL display tube data (Grid)	Bit 9
17	P1	P10	FSA	O	*	FL display tube data (Anode)	Anode A
18		P11	FSB	O		FL display tube data (Anode)	Anode B
19		P12	FSC	O		FL display tube data (Anode)	Anode C
20		P13	FSD	O		FL display tube data (Anode)	Anode D
22	P2	P20	FSE	O	*	FL display tube data (Anode)	Anode E
23		P21	FSF	O		FL display tube data (Anode)	Anode F

Table 2-4-1A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

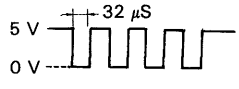
Pin No.	Port name		Signal name	I/O	Initial value	Description
24	P2	P22	FSG	O	*	FL display tube data (Anode) Anode G
25		P23	FSH	O		FL display tube data (Anode) Anode H
26	K0	K00	KS0	I	*	Key matrix input data Bit 0
27		K01	KS1	I		Key matrix input data Bit 1
28		K02	KS2	I		Key matrix input data Bit 2
29		K03	KS3	I		Key matrix input data Bit 3
35	R8	R80	$\overline{IRQ}$	I/O	1	I/0 for control signal of data transmission/reception with IC15 (X32 board). Outputs the interrupt pulse signal to IC15 (X32) when data is transmitted. Receives the interrupt pulse signal generated by IC15 (X32) after completion of data reception.
36		R81	FSEL	I	1	Input for A-PAUSE/M-SCAN selection signal. Selects the A-PAUSE function at "H", and the M-SCAN function at "L".
37		R82	$\overline{REM}$	I	1	Input for remote control signal. This signal is input in the PPM system using NEC remote control IC μPD1943G. Reception processing is made in its reading edge.
38		R83	TP	I/O	1	TP input: Input for timer play selection signal. At "H", timer play function turns OFF. CHIRP output (Not connected): Output for chirp sound control signal. Becomes "H" for approx. 0.072 sec after pressing the key.
39	R9	R90	DAT12	I/O	1	I/0 for control signal of data transmission/reception with IC15 (X32). Works for transmission of data signal from IC15 (X32) to IC1 (X25-2020).
40		R91	DAT21	I/O	1	I/0 for control signal of data transmission/reception with IC15 (X32). Becomes "H" during transmission of data signal from IC15 (X32) to IC1 (X25-2020). In reverse communication, works for transmission of data signal from IC1 (X25-2020) to IC15 (X32).
41		R92	$\overline{SCK}$	I/O	1	I/0 for control signal of data transmission/reception with IC15 (X32).  Shifts the shift lock signal for data reception (two-way) in units of 4 bits at a time.

Table 2-4-1A

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin No.	Port name		Signal name	I/O	Initial value	Description
21			V_{SS}	Power supply		Power supply (0 V)
30		—	TEST	I		Not used (Connected to V_{SS})
31			X_{IN}	I		OSC connection pin
32			X_{OUT}	O	—	OSC connection pin
33			$\overline{\text{RESET}}$	I		Initialize signal input
34			$\overline{\text{HOLD}}$	I		Not used (Connected to V_{DD})
42			V_{DD}	Power supply		Power supply (+5 V)

Table 2-4-1A

Operation of IC1 (TMP47C41N) display board X25-2020-00

1) Different display divisions...Key scan and key sense section

TMP47C41N (IC1), a CMOS version of TMP4740N (IC15 NMOS), has the same function as TMP4740N except that it has 1/2 the execution speed. In addition provided with 20 pins of high dielectric strength output ports, it is capable of directly driving the FL display tube without driver.

A total of 83 elements; the 9-digit FL display tube (which consists of 8 digit number display units, 11 mode display lamps and 16 channel display lamps) are dynamically driven by IC1 (TMP47C41N). Table 2-4-1B shows the display matrix of the FL display tube.

Pins FSA-FSK correspond to anode segments a to k of FL display tube and pins FD1 to FD9 to the grid pins of the respective display digits. For key scan, 1033.6 Hz obtained from 4096-division of the reference clock signal frequency 4.2336 MHz is used as the scan frequency. The system in which scan is made to grid G9 alone twice in one cycle is employed because of wide display area, etc. Accordingly, scan to total 10 digits is made, and the effective scan frequency per digit is 103.4 Hz. This scan to the 10 digits is performed in the order of 1st digit (FD1) → 2nd digit (FD2) → 3rd digit (FD3) → 4th digit (FD4) → 9th digit (FD9) → 5th digit (FD5) → 6th digit (FD6) → 7th digit (FD7) → 8th digit (FD8) → 9th digit (FD9), in which the amount of change in the brightness of each digit is suppressed low. Fig. 2-4-1B shows the operation timing for each segment and each digit, and Table 2-4-1C shows the main function of each display division.

This system has 24 non-lock type mechanical keys. The non-lock type keys are arranged in a key matrix, as shown in Fig. 2-4-1C.

For key scan to the key matrix shown in Fig. 2-4-1C, digit pulses (FD4 ~ FD9) are used as key matrix scanning pulse.

In addition, after pressing a key except the timer standby switch, an "H" signal appears at port pin R83 (CHIRP) during approx. 0.072 sec.

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

▼	▼	▼	▼	▼	▼	▼	▼		FSK (R52)
CH-2	CH-4	CH-6	CH-8	CH-10	CH-12	CH-14	CH-16	PAUSE (LED)	FSJ (R51)
▼	▼	▼	▼	▼	▼	▼	▼	PLAY (LED)	FSI (R50)
CH-1	CH-3	CH-5	CH-7	CH-9	CH-11	CH-13	CH-15	REPEAT	FSH (P23)
Address display TNO Upper Lower		Address display X Upper Lower		Address display MIN Upper Lower		Address display SEC Upper Lower		+ TOTAL	FSG (P22)
								M-SCAN	FSF (P21)
								− RE-MAINING	FSE (P20)
								M-PLAY	FSD (P13)
									FSC (P12)
								DISC	FSB (P11)
								DATA	FSA (P10)

Display data

FD 1 (R53)	FD 2 (R60)	FD 3 (R61)	FD 4 (R62)	FD 5 (R63)	FD 6 (R70)	FD 7 (R71)	FD 8 (R72)	FD 9 (R73)

Display digit scan bits

Fig. 2-4-1B Display matrix in FL tube display section

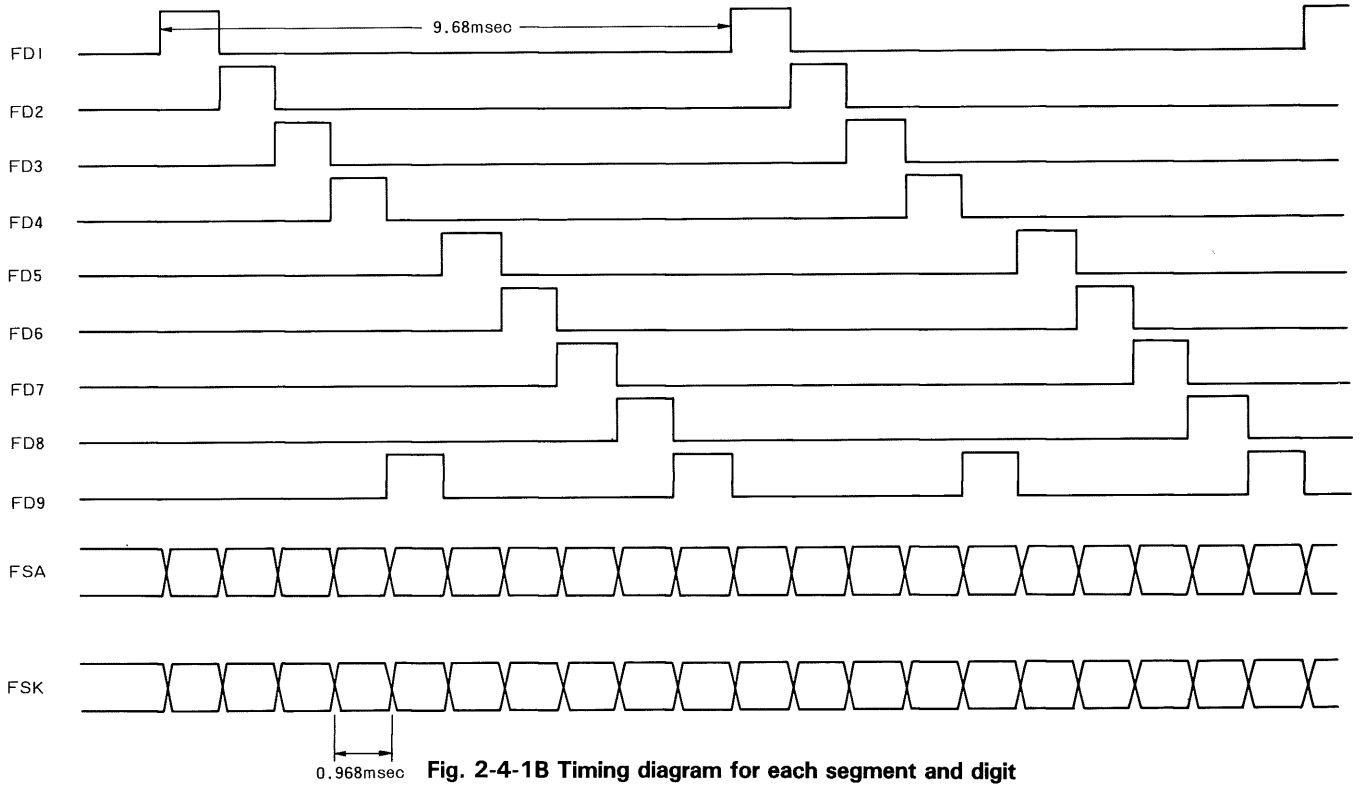


Fig. 2-4-1B Timing diagram for each segment and digit

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Lamp name	Main function
Display section	8-digit number display division. Normally, displays the address data during play. The respective pairs of 2 digits from the left show TNO, X, MIN, and SEC in order. However, when the tray is opened, all digits go off. In addition, when a numeral key or the M-READ key is operated, TNO and X (X may not be displayed) alone are displayed, and MIN and SEC are blanked. Then, during search, TNO and X (X may not be displayed) blink, and MIN and SEC go off. The display format is shown below: 0 1 2 3 4 5 6 7 8 9

Table 2-4-1C

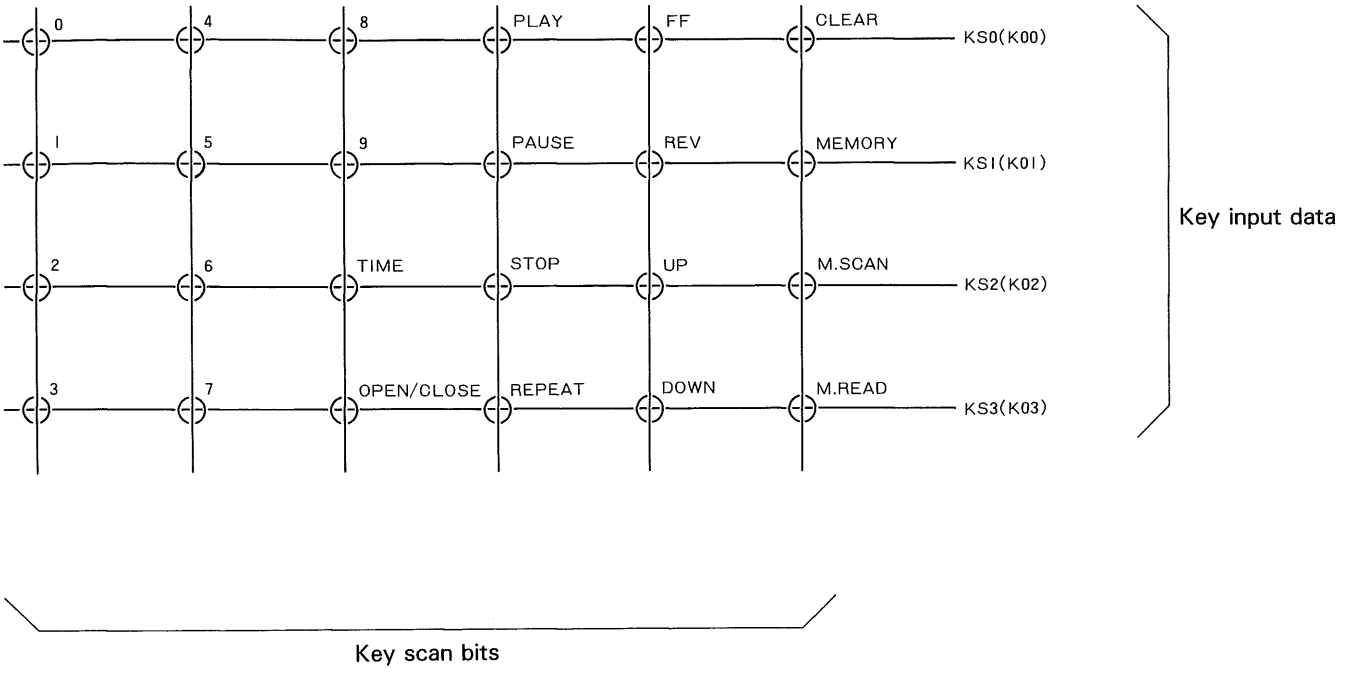
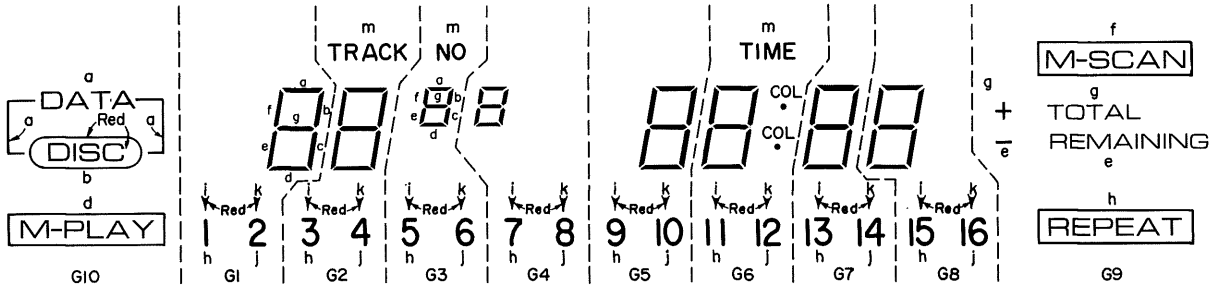


Fig. 2-4-1C Simplified diagram of key matrix



PIN ASSIGNMENT

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Assignment	F	P_m	P_a	P_b	P_c	P_d	P_k	P_j	P_i	G1	G2	G3	G4	G5	G6	G7	G8	G9 G10	P_h	P_e	P_g	P_{COL}	P_f	F

Fig. 2-4-1D

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Digit				FD 4 (R62)				FD 5 (R63)				FD 6 (R70)			
Port name		Signal name	Pin No.	11				12				13			
	K00	KS 0	26	1	0	0	0	1	0	0	0	1	0	0	0
K 0	K01	KS 1	27	0	1	0	0	0	1	0	0	0	1	0	0
	K02	KS 2	28	0	0	1	0	0	0	1	0	0	0	1	0
	K03	KS 3	29	0	0	0	1	0	0	0	1	0	0	0	1
Accept key				0	1	2	3	4	5	6	7	8	9	TIME	OPEN CLOSE

Digit				FD 7 (R71)				FD 8 (R72)				FD 9 (R73)			
Port name		Signal name	Pin No.	14				15				16			
	K00	KS 0	26	1	0	0	0	1	0	0	0	1	0	0	1
K 0	K01	KS 1	27	0	1	0	0	0	1	0	0	0	1	0	0
	K02	KS 2	28	0	0	1	0	0	0	1	0	0	0	0	0
	K03	KS 3	29	0	0	0	1	0	0	0	1	0	0	1	1
Accept key				PLAY	PAUSE	STOP	REPEAT	FF	REV	UP	DOWN	CLEAR	ME-MORY	M·READ	ALL CLEAR

Fig. 2-4-1E Key matrix input when key is pressed

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2) Remote control reception data processing

The remote control transmitter in this system, in which the key matrix shown in Fig. 2-4-1F is connected to remote control transmission IC μPD1943G, performs signal transmission in PPM (Pulse Position Modulation) by infrared LEDs. Reception data processing is made by the light receiver circuit. The PPM signal received by photo diode (PH302B) is amplified, waveform-shaped and fed to pin R82 of IC1 (X25) to be transduced to electrical signal. Fig. 2-4-1G shows the reception signal format from the remote control transmitter.

When a key is pressed, the leader code with 9 msec "L" period and 4.5 msec "H" period is input first. This code is used for the preparation pulse indicating that data will be received from this time on. Next, total 32 bits are input, which include custom code (8 bits), inversion code (8 bits) of the custom code, data code (8 bits) and inversion code (8 bits) of the data code.

Code bits "0" and "1" are distinguished by periodical length shown in Fig. 2-4-1G. In addition, when a key is pressed continuously, the output after 108 msec does not become the same code as before. Thus, leader codes alone, each with 9 msec "L" period and 2.25 msec "H" period, appear continuously.

In this system, the falling edge of the reception signal is detected by interrupt function (INT1) of IC1 (TMP47C41N) and then the time till the next falling edge is measured. Thereby, the codes and data mentioned previously are recognized.

The above time measurement is made by counting internal pulses in the internal timer, in which internal pulse appears every 0.242 msec periodically. Here, the value from dividing the time corresponding to each code or data by 0.242 msec, i.e., the number of internal pulses, is shown below:

Data "0" = 1.125 msec → 4.7
Data "1" = 2.25 msec → 9.3
Leader code = 13.5 msec → 55.8
When key is pressed continuously = 96.19 msec → 397.5

From this point, this system sets each code or data according to the number of internal pulses as follows:

Number of internal pulses
1 to 6 .....data "0"
7 to 17 .....data "1"
416 or more .....key released
Others .....New CODE reception start

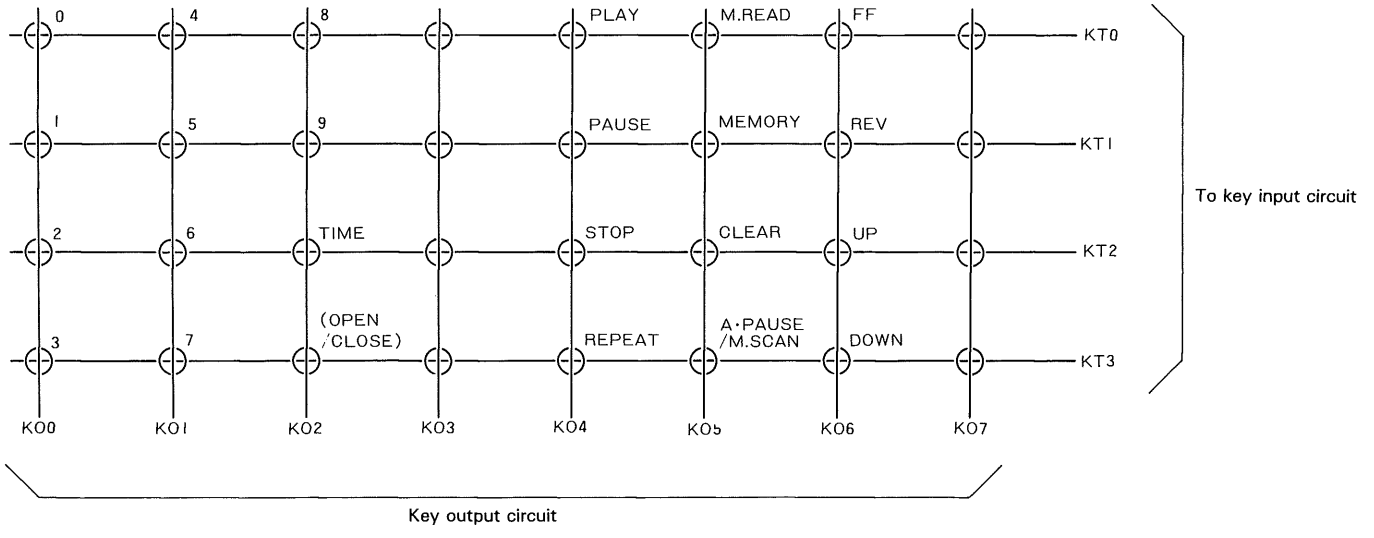


Fig. 2-4-1F Simplified diagram of key matrix in remote control transmitter

2. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

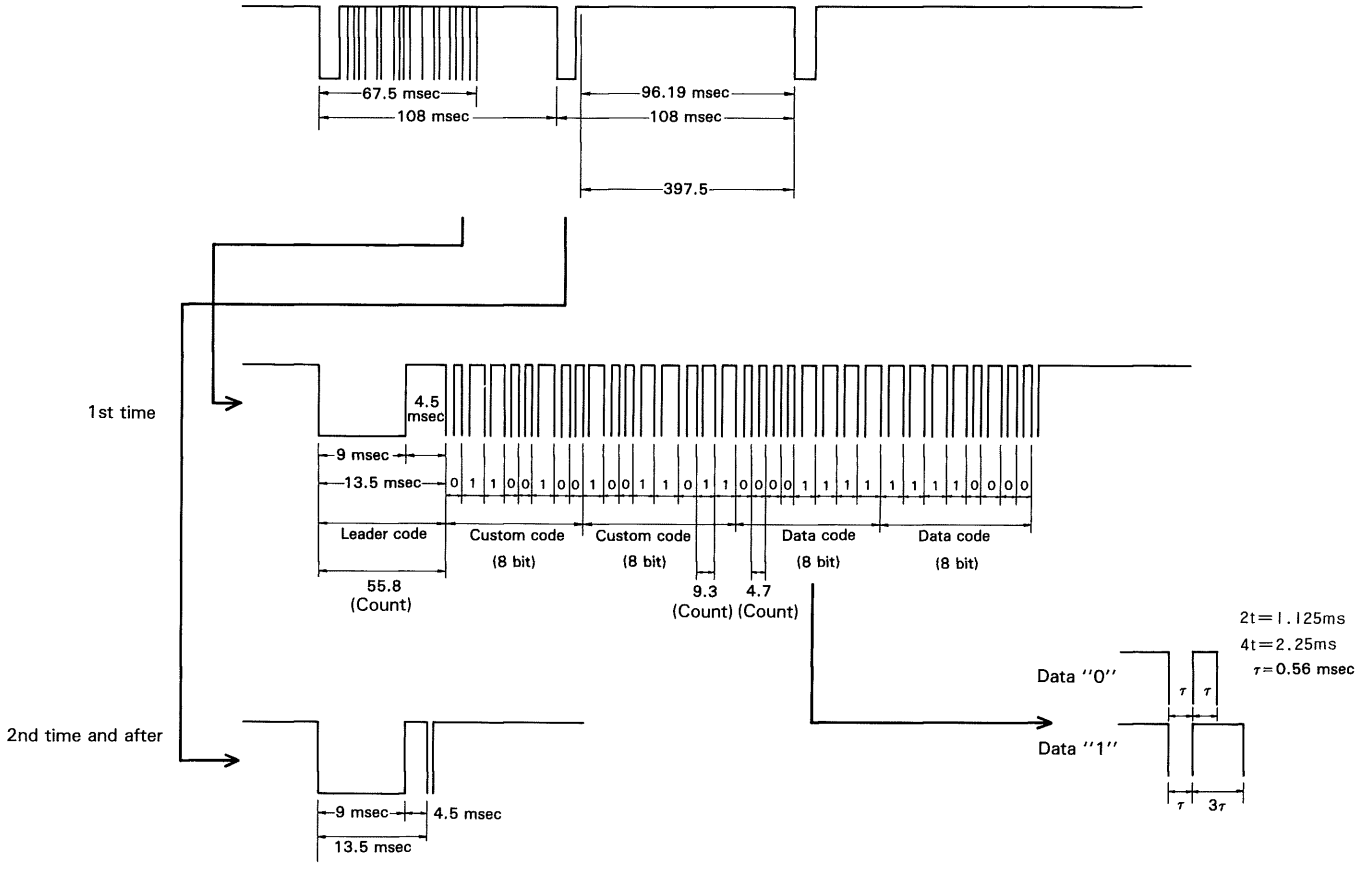


Fig. 2-4-1G

3. OPERATION OF MAIN MICROPROCESSOR

3-1 OPERATION OF CPU 1 (IC15)

CPU 1 (main microprocessor) has many roles. The following describes the main ones.

3-1-1 Tray close operation

The microprocessor sends a mechanism control instruction to servo PCB IC15 (TC15G) and performs this operation while monitoring the mechanism condition by switches. Fig. 3-1A shows the operation flow chart.

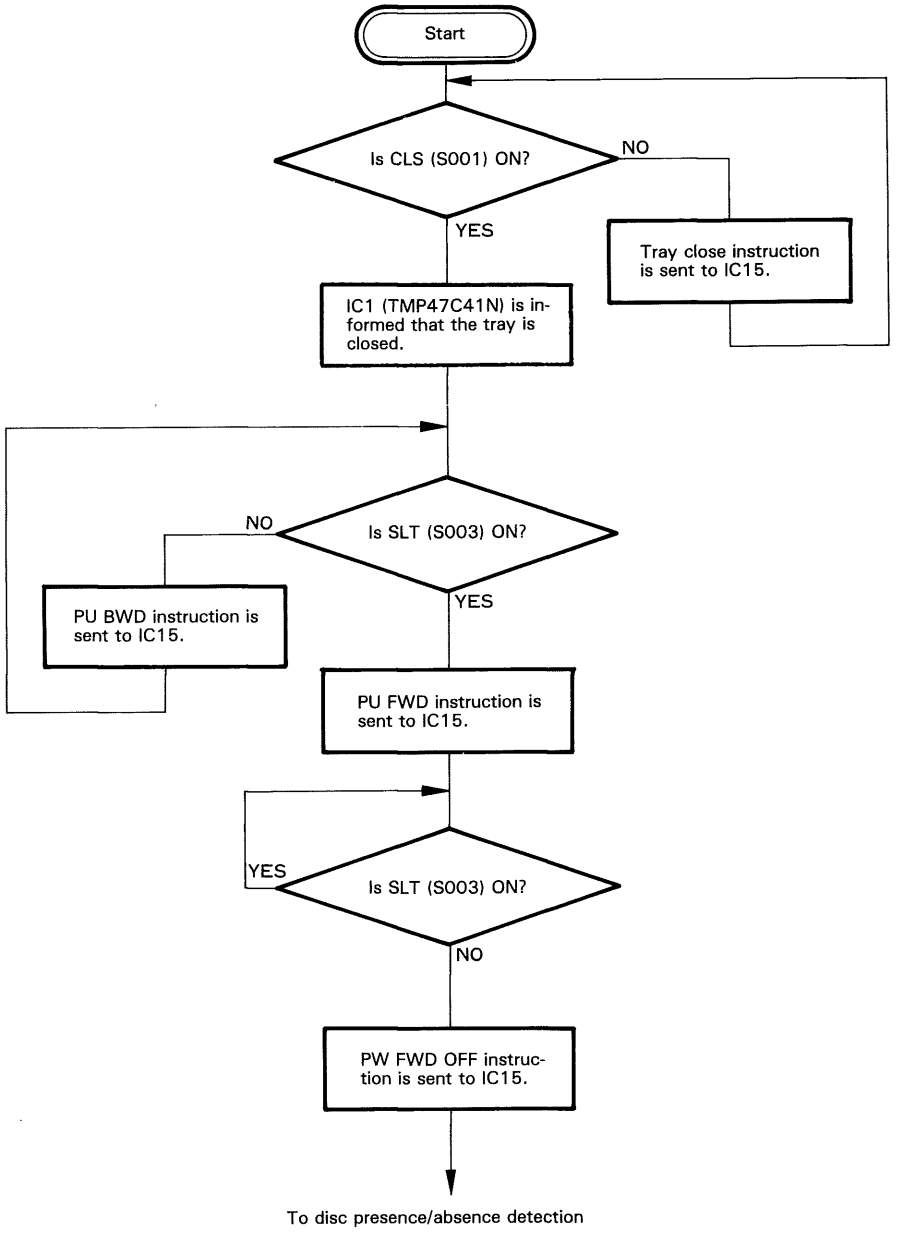


Fig. 3-1A Operation flow chart

3. OPERATION OF MAIN MICROPROCESSOR

3-1-2 Disc presence/absence detection

With a disc on the tray, when the laser beam is just focused, pin DOK of CN2 becomes "L" so this detection can be made. The pickup lens is moved forwards and backwards by signal FSRCH (2.5 Hz) to search for the focusing point. Thus, when pin DOK does not become "L" even after 2 cycles of this signal, the microprocessor judges that no disc is present.

3-1-3 Disc surface/rear judgement

Fig. 3-1B shows the operation flow chart. Words at the left of some steps denote pin names of IC15.

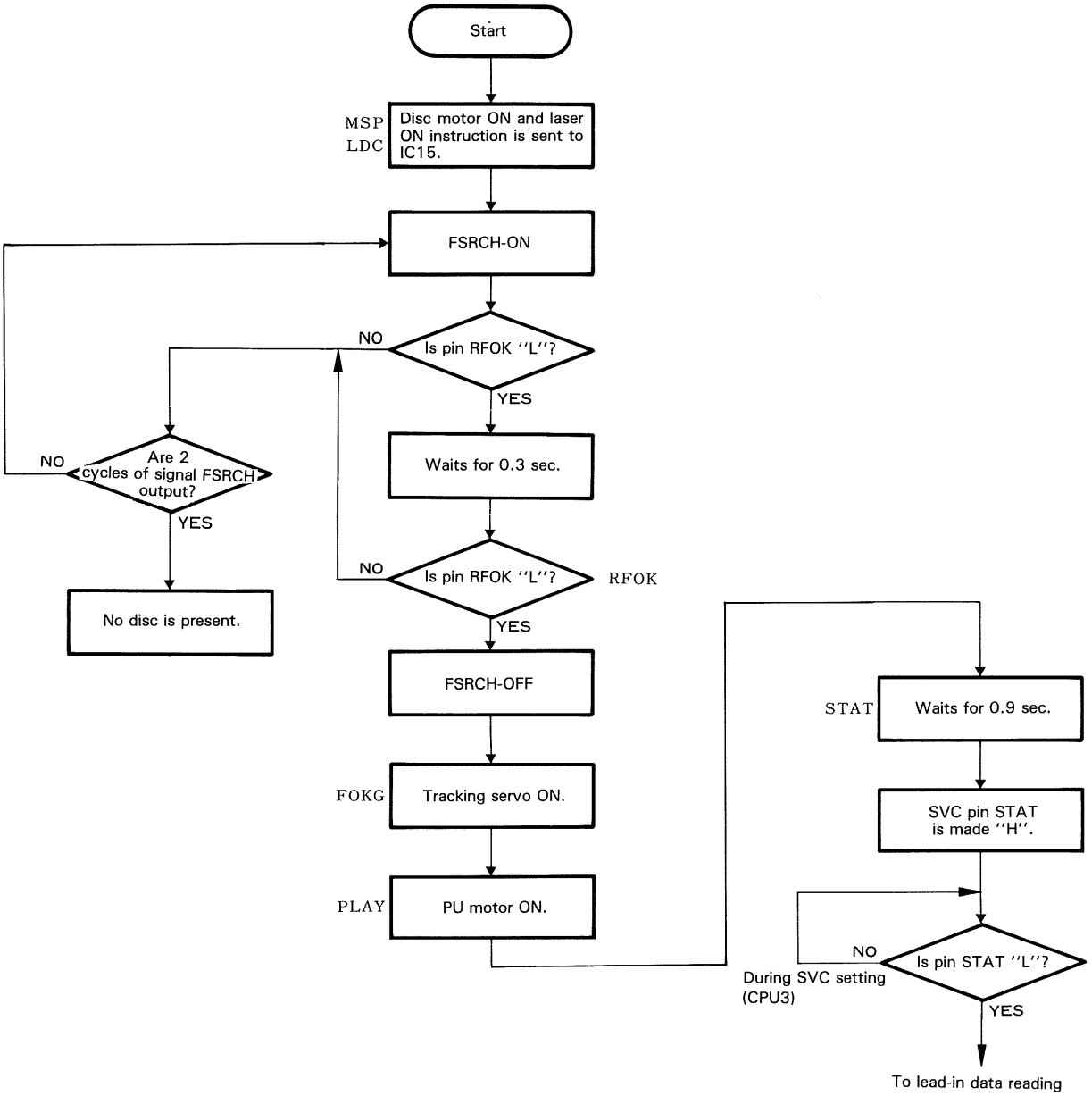


Fig. 3-1B Operation flow chart

3. OPERATION OF MAIN MICROPROCESSOR

3-1-4 Lead-in data reading section

Before lead-in data reading operation, the pickup is located at the point at which switch SLT (S003) is turned OFF by tray close operation. This point refers to the beginning of the disc program area. The pickup is moved backwards about 2 ~ 3 mm from this point to the center of the disc lead-in area by backward kick operation and lead-in data reading starts.

When reading cannot be completed even after approx. 20 sec, reading is stopped and operation shifts to search operation of the first tune. In this case, dynamic search and computation of various times performed based on TOC data become impossible. Fig. 3-1C shows the operation flow chart.

Note: TOC... Table of Contents

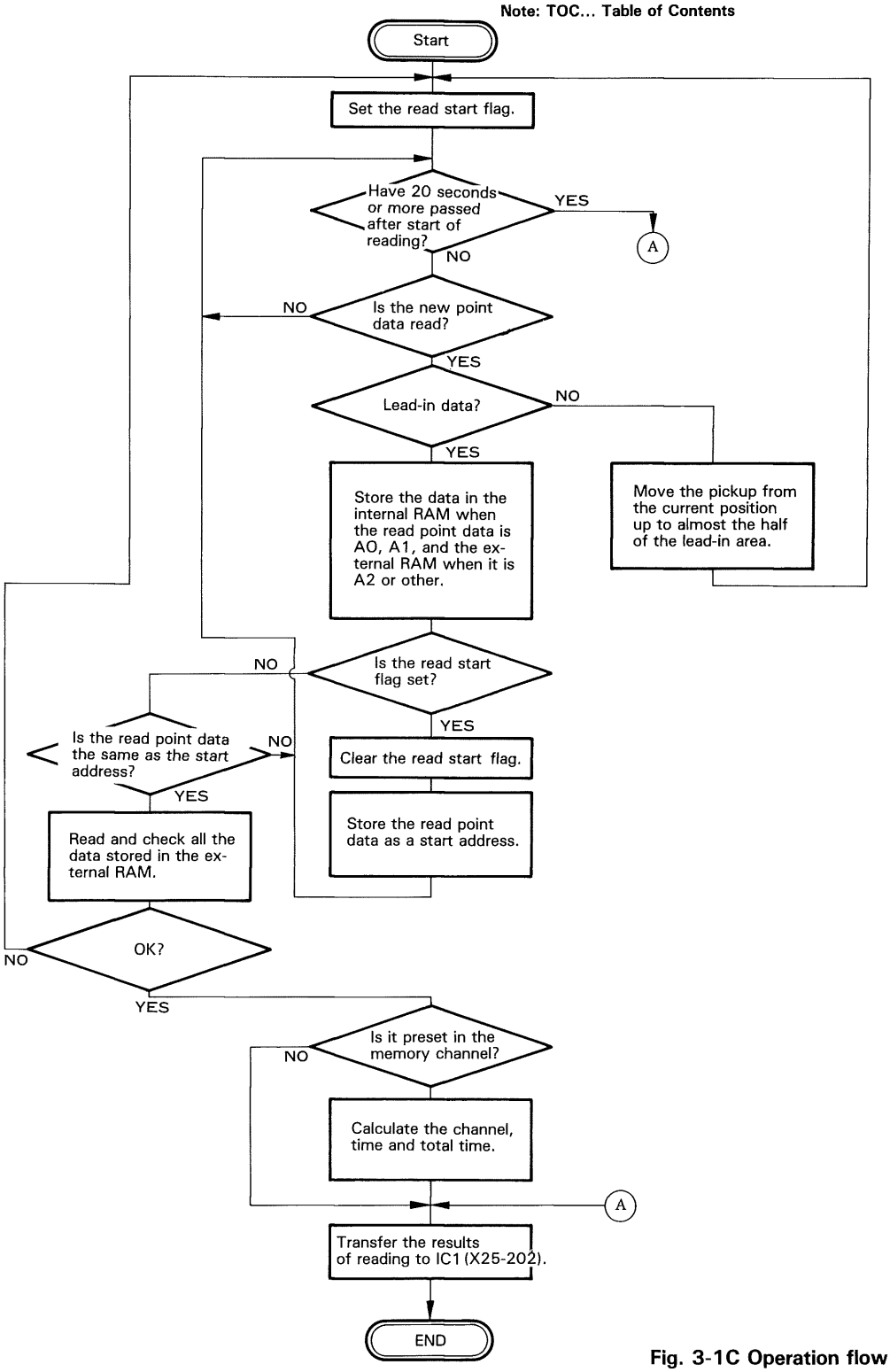


Fig. 3-1C Operation flow chart

3. OPERATION OF MAIN MICROPROCESSOR

3-1-5 Address data (data Q, time data) reading

In conformity with the standard for CD system, time data is recorded as channel Q data by use of 1 bit out of the 8 bits which come after the sync signal of frame data. 98 of these channel Q signal in 7350 Hz frame signal can be used as meaningful time data. Thus, this data appears repeatedly at 7350Hz/98 = 75 Hz.

For the address data format, refer to the address data configuration shown below.

In DP-1100B/II, the time data read out is recorded and held by 20 words (1 block) in units of 4 bits in EFM signal decoder(IC8) TC9178F. The data in a block is read by 20 reading operations in units of 4 bits on the program.

Fig. 3-1D shows the operation flow chart.

The address data format (in the program area) is as shown below.

S0, S1 : 2-bit address signal synchronizing pattern

CONTROL : 4-bit control data. Selection of 2CH/4CH play signals.
Designates pre-emphasis ON/OFF and digital copy enable/disable.

	0	0	

0	0	X	0	2CH, Emphasis OFF
1	0	X	0	4CH, Emphasis OFF
0	0	X	1	2CH, Emphasis ON
1	0	X	1	4CH, Emphasis ON

0	X	Digital copy disable
1	X	Digital copy enable

ADR : 4-bit mode data
- MODE 1 (BCD 1) : Address mode
- MODE 2 (BCD 2) : Disc catalog number mode
- MODE 3 (BCD 3) : Special information mode (Written by 0 to 9 and A to Z alphanumeric characters)

MNR : Music number expressed by 2-digit BCD (8 bits)

X : Index in each music expressed by 2-digit BCD (8 bits)

MIN : Elapsed time (minute) in each music expressed by 2-digit BCD (8 bits)

SEC : Elapsed time (second) in each music expressed by 2-digit BCD (8 bits)

FRAME : Elapsed time (frame) in each music expressed by 2-digit BCD (8 bits) (1 frame = 1/75 seconds)

ZERO : Unused (8-bit 0 data)

AMIN : Elapsed time (minute) in disc expressed by 2-digit BCD (8 bits)

ASEC : Elapsed time (second) in disc expressed by 2-digit BCD (8 bits)

FRAME : Elapsed time (frame) in disc expressed by 2-digit BCD (8 bits)

CRC : 16-bit CRC (Cyclic Redundancy Check) code data calculated for CONTROL - A FRAME data

S_0,S_1	CONTROL	ADR	MNR	X	MIN	SEC	FRAME	ZERO	AMIN	ASEC	AFRAME	CRC	S_0,S_1	---
2	4	4	8	8	8	8	8	8	8	8	8	16 bits		

Address data configuration

3. OPERATION OF MAIN MICROPROCESSOR

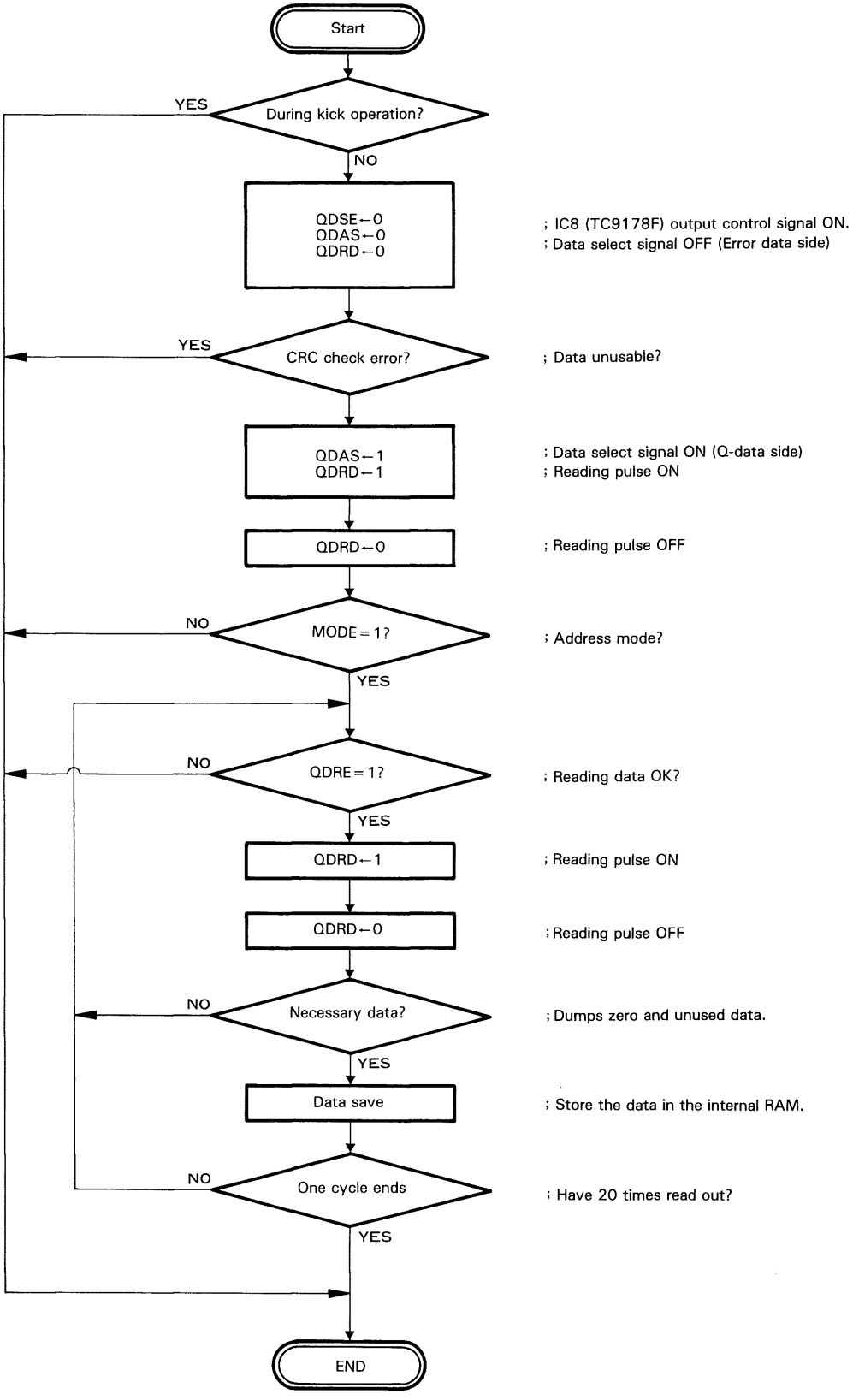


Fig. 3-1D Q-data reading flow chart.

3. OPERATION OF MAIN MICROPROCESSOR

3-1-6 FF/REV mode

When the FF key is pressed, fast forward pickup carry operation is made, while when the REV key is pressed, fast backward pickup carry operation is made. In the case of continuous key pressing, the fast forward/backward pickup carry speed is varied according to the mode (play or pause) just before pressing of the FF/REV key.

Table 3-1A describes this variation. In addition, continuous forward/backward pickup carry operation is all performed by actuator kick.

Mode before key pressing / Key pressing time	Play mode	Pause mode
Simple pressing of less than 0.5 sec.	Kick forward/backward carry operation equivalent to 1 sec play time	←
Cotinuous pressing of more than 0.5 sec	Kick forward/backward carry operation equivalent to 2 sec play time every period of 200 msec (10 times the normal speed)	Kick forward/backward carry operation equivalent to 10 to 20 sec play time every period of 200 msec (50 to 100 times the normal speed)

Table 3-1A

As seen from this table, in the case of single key pressing of less than 0.5 sec, kick operation equivalent to 1 sec play time is made in both play and pause modes. But, in the backward carry operation in play mode, a kick operation equivalent to about 1.5 sec play time is made for the backward carry equivalent to obtain 1 sec play time from the time when the key had been pressed.

After the kick operation equivalent to 2 sec play time in continuous key pressing of more than 0.5 sec in play mode, muting is released until the next kick operation starts. In this way, operability is improved with what is called cue/ review operation.

In simple key pressing of less than 0.5 sec and continuous forward/backward feed operation in play mode, the pickup feed speed is almost constant even when the FF/REV key is pressed in any pickup position on the disc by use of the method described in the following.

That is, the disc is separated into divisions of 10 minutes by the absolute time, and the data of the average number of tracks/sec in each division is stored in ROM table. Thereupon, when kick operation is made, the absolute time of the disc is read out from data Q, and the data of the number of tracks/sec in that pickup position is read out. Then, based on this data, the required kick amount (1 or 2 sec) is attained by combination of 1, 3, 5, 7 and 15 kicks. Continuous forward carry operation in pause mode cannot be made by this method since the amount of pickup carry at a time is too much.

To compensate this, a kick operation is made to move the pickup 60 tracks every period of 200 msec wherever the pickup is located on the disc. Therefore, the forward/backward carry speed in the disc inside is about twice that in the disc outside.

Kick operation is all performed by semi-custom LSI IC15 (T7001-0007 or TC15G0008AP). For this purpose, the microprocessor outputs kick data (kick amount, kick direction) to semi-custom LSI IC15. Then, when TTAC signal of the kick operation completion signal from IC15 or RFG signal is input to IC15 of processor pcb, IC15 of servo pcb, stops output of kick data and changes to the next kick operation or other operation mode.

Table 3-1B shows the kick data output to IC15 (T7001-0007 or TC15G008AP).

3. OPERATION OF MAIN MICROPROCESSOR

3-1-7 Search operation

The search system whose aim is to assure accurate music scan in a short required time is a combination of two systems: dynamic search system in which the pickup is carried at high speed based on the TOC data, and kick search system in which the pickup is carried at high precision by kick operation based on the address data until completion of the required address retrieval. The purpose of search is to find the begining of the program, also the data designation of TNO and X is possible.

First, the dynamic search system is described. In the ROM area in IC15 (TMP4740N), a table by which the elapsed time (absolute time) of the disc is converted to a positional value in the radius direction of the disc is prepared.

This conversion table has the positional data calculated from track pitch (1.6 μm) and linear velocity (1.2 m/sec), in which the pickup position in the radius direction is represented by the number of tracks from the start point of the program area.

DP-1100/B has a conversion table in which the number of tracks against the absolute time in units of 10 minutes and the average number of tracks/minute in each unit of 10 minutes are written. In addition, in external RAM IC14 (TC5514P), the play start absolute time of each tune recorded in the disc is stored. **Thus, in the dynamic search system, the time difference between the absolute address of the searching program read out from the external RAM and the present absolute address is converted to the difference in number of tracks by the conversion table, and at the same time, the ripple of the RF signal generated when the pickup carried at high speed goes across tracks is counted. Thereby, it judges whether or not the pickup is carried by the required number of tracks.** Fig. 3-1E shows the operation flow chart of the dynamic search system. Further description is made following this chart.

MODE 4 (R50)	MODE				Control Code	
	0 (R40)	1 (R41)	2 (R42)	3 (R43)		
0→1	0	0	0	0	0	KICK RESET
	1	0	0	0	1	KICK RESET
	0	1	0	0	2	BWD 1 TRACK KICK
	1	1	0	0	3	FWD 1 TRACK KICK
	0	0	1	0	4	BWD 3 TRACK KICK
	1	0	1	0	5	FWD 3 TRACK KICK
	0	1	1	0	6	BWD 5 TRACK KICK
	1	1	1	0	7	FWD 5 TRACK KICK
	0	0	0	1	8	BWD 7 TRACK KICK
	1	0	0	1	9	FWD 7 TRACK KICK
	0	1	0	1	A	BWD 15 TRACK KICK
	1	1	0	1	B	FWD 15 TRACK KICK
	0	0	1	1	C	BWD 31 TRACK KICK
	1	0	1	1	D	FWD 31 TRACK KICK
	0	1	1	1	E	BWD CONTINUOUS
	1	1	1	1	F	FWD CONTINUOUS

Table 3-1B

* Before output of the kick data, the tracking servo is turned OFF (at Mode 4 (port pin R50) = 0.... control code 8 is output in backward kick and control code B in forward kick). After that, kick data is output to Mode 0 to 3 (port pins R40 to R43) to make Mode 4 (port pin R50) = 1.

3. OPERATION OF MAIN MICROPROCESSOR

[1] The play start absolute time A1 (min, sec) of the searching program is read out from external RAM IC14 (TC5514P).

[2] The present address (absolute time) is taken as A2 (min, sec).

[3] The difference between the searching position and the present position, $\Delta A = |A1 - A2|$ (min, sec) is calculated.

[4] Each of the following processes is performed depending on the amount of ΔA.

[5.1] When ΔA is more than 1 min.:
A1 and A2 are converted to numbers of tracks, T1 and T2 by use of the conversion table. Then, the number of tracks to the searching position, $\Delta T = T1 - T2$, is calculated.

[5.2] When ΔA is 10 to 59 sec.:
The number of tracks, ΔT, is determined depending on ΔA.

[5.3] When ΔA is less than 10 sec.:
Search is performed in the kick search system explained later.

[6] ΔT is converted to a number with a base of 64, which is then set to internal counter EC1 in IC15 (TMP4740N). For example, when ΔT is 512 tracks, $512/64 = 8$ is set.

[7.1] When ΔT is a plus number, i.e., when search is performed in the direction of the disc edge, FWD-search mode (Code 7) is output to semi-custom IC15 (T7001 — 0007 or TC15G0008AP) to turn ON the pickup motor. Then, FWD-continuous kick mode (Code F <KICK>) is output to start kick operation.

[7.2] When ΔT is a minus number, i.e., when search is performed in the direction of the disc center, BWD-search mode (Code 6) is output and then BWD-continuous kick mode (Code E <KICK>) is output to start kick operation like step (7.1).

[8] Judges whether or not the pickup is carried by the required number of tracks. In semi-custom IC15 (T7001 — 0007 or TC15G0008AP), when continuous kick operation is started, the number of tracks by which the pickup is carried is counted and signal TTAC is inverted each time the pickup is carried 32 tracks. IC15 (TMP4740N) has an event counter function to detect the rising edge of the pulse input from outside to perform count-up operation. In this system, signal TTACK is input as count pulse to IC15 (TMP4740N), with which the count value in its internal counter EC1 is raised.
Thus, kick operation is performed until EC1 counts up to the number set at step [6] to carry the pickup by the required number of tracks.

[9] Brake operation is made to stop the pickup in a short time.
Fig. 3-1F shows this operation timing chart.

3. OPERATION OF MAIN MICROPROCESSOR

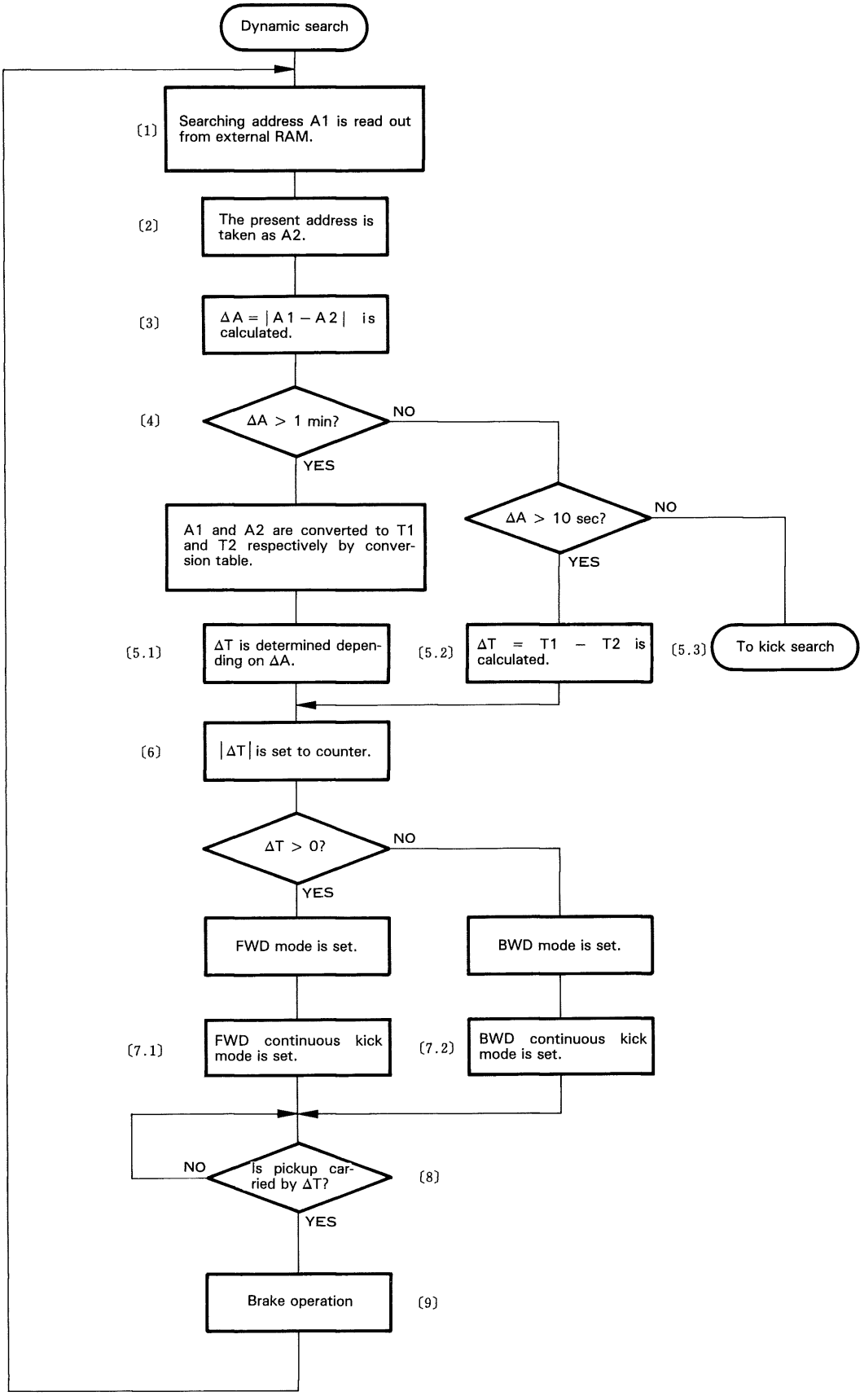


Fig. 3-1E Operation flow chart of dynamic search system

3. OPERATION OF MAIN MICROPROCESSOR

When ΔT is more than 512 tracks, considering the effect of disc eccentricity and brake operation, ΔT + 2 (128 tracks are added; refer to Table 3-1D) is calculated and a kick operation in which the pickup is carried by more than the calculation value is performed. On the other hand, when ΔT is less than 512 tracks and if the above same method is performed, the difference between the required number of tracks and the number of tracks by which the pickup is actually carried is very large. To compensate this, the operation shown in Fig. 3-1G is made, i.e., kick operation by which the pickup is carried by 31 tracks is executed in intervals of 3 msec repeatedly. The upper limit in the number of repetitions depends on the performance of external circuit. Since the performance of external circuit may be greatly changed hereafter, the maximum number of repetitions is controlled by varying the inputs to port pins $KMAX_0$ and $KMAX_1$ (only immediately after power ON). The following table shows the relationship between the maximum number of repetitions and these inputs.

$KMAX_0$	$KMAX_1$	Maximum repetitions
0	1	4
1	0	8
1	1	6

Table 3-1C

The dynamic search system, based on TOC data, can be executed only when TNO alone is designated as the searching program No.(X = 01 is designated). Therefore, when X is also designated, dynamic search operation which is a little different from the system based on TOC data is executed. The difference is that after the searching program No. and the present program No. coincide, kick search operation takes place. For example, when TNO = 3 and X = 8 are designated for the searching program, dynamic search operation to TNO = 3 is performed and the pickup is moved at high speed to within the third program area, after which kick search operation is executed.

In addition, when TOC data is not read out, dynamic search operation cannot be performed. In this case, therefore, all search operation is performed in the kick search system.

Against this case, in DP-1100B/II, a self-learning function of TOC data is produced by writing in external RAM the absolute time on completion of search operation so that the subsequent search operation can be performed promptly.

Next, **the kick search system** is described.

In this system, search operation is performed based on only the address data read out.

Here, the amount of pickup movement is converted to the number of tracks which is represented by stage No. Normally, at first, operation begins with the greatest amount, then the amount is lowered according to the searching program and the pickup is moved in the backward direction. This process is performed repeatedly. Thus, the amount of pickup movement is controlled so that the kick operation is necessarily completed before the searching program.

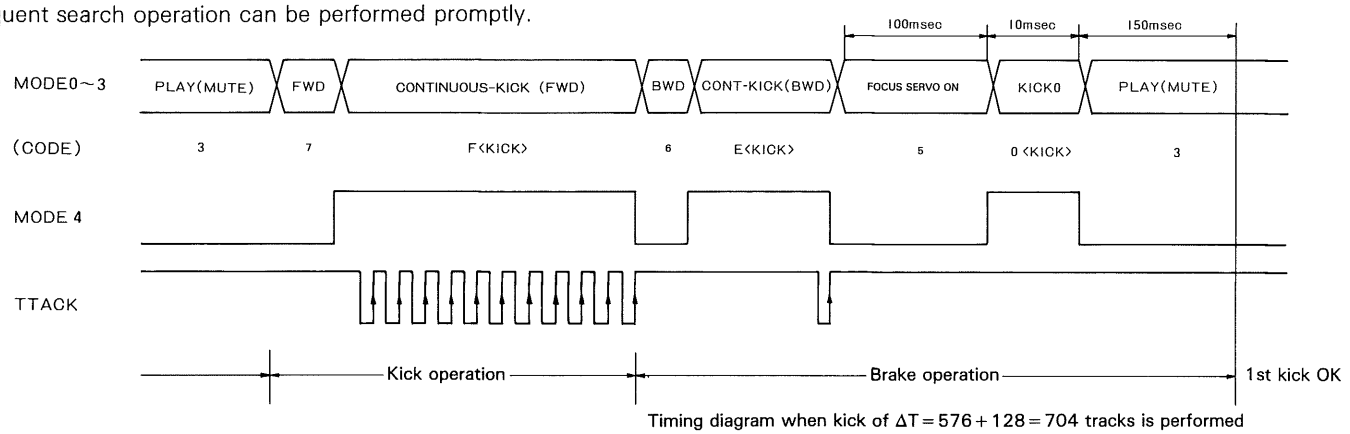
In DP-1100B/II, 9 stages for amount of pickup movement are set as shown on Table 3-1D.

Stage	Set number of tracks (pickup movement time conversion value (sec))
1	1 track (0.33 ~ 0.12)
2	3 tracks (1 ~ 0.4)
3	5 tracks (1.7 ~ 0.6)
4	7 tracks (2.3 ~ 1)
5	15 tracks (5 ~ 2)
6	31 tracks (11 ~ 4)
7	64 tracks (21 ~ 8)
8	128 tracks (43 ~ 16)
9	256 tracks (85 ~ 32)

Table 3-1D Relationship between stages and set numbers of tracks

In the table, concerning play time conversion value, the value at the left in the parenthesis represents the time required to move the number of tracks at the outer-most side of disc and the value at the right is for the inner-most side. For the operation, the code (2 <KICK> to D <KICK>) corresponding to each stage is output to semi-custom IC15 (T70001 — 0007 or TC15G0008AP). Stages 7 to 9 are executed by repeatedly performing a kick operation which moves the pickup 31 tracks and twice the 1 track kick.

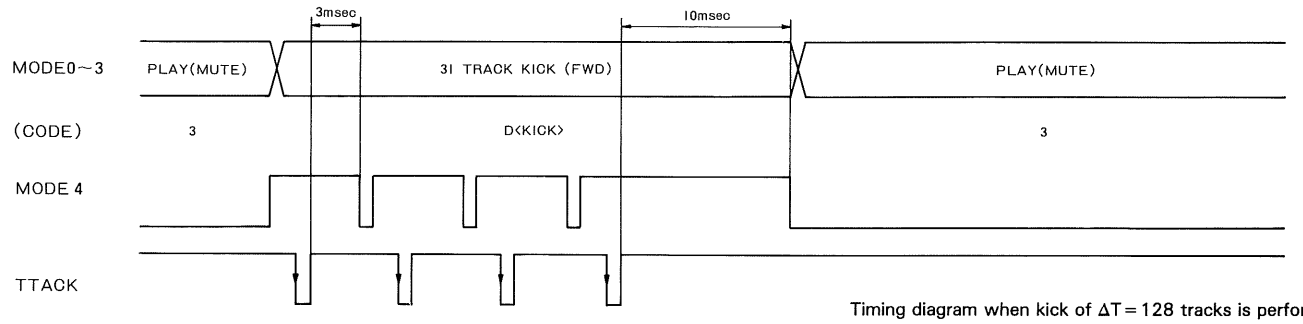
For example, stage 7 (64 tracks) is executed by performing twice a kick operation which moves the pickup 31 tracks and twice the 1 track kick.



Timing diagram when kick of ΔT = 576 + 128 = 704 tracks is performed

Fig. 3-1F

3. OPERATION OF MAIN MICROPROCESSOR



Timing diagram when kick of ΔT = 128 tracks is performed
Timing diagram of dynamic search system

Fig. 3-1G

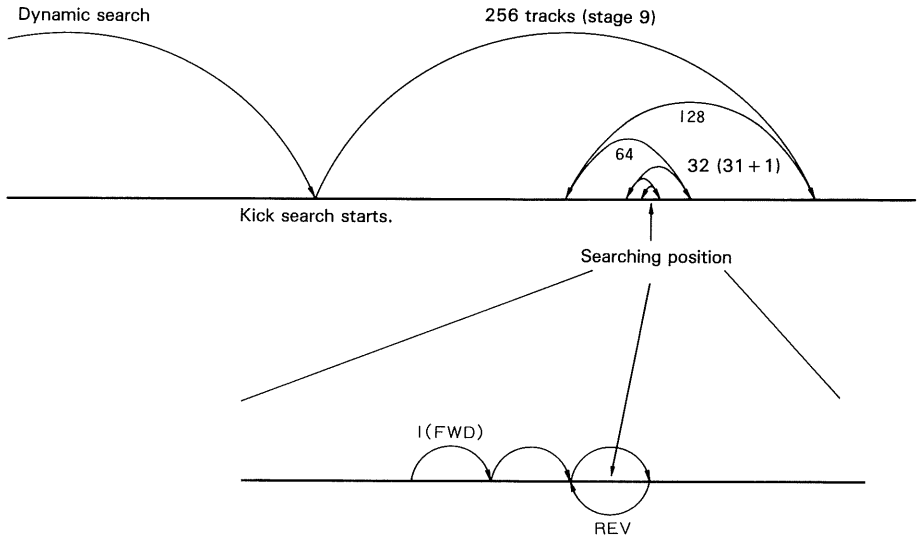


Fig. 3-1I Operation model of kick search system

Fig. 3-1H shows the operation flow chart of the kick search system. Further description is made following this chart.

[1] The stage No. in which kick search operation starts is determined according to the time difference between the present absolute address and the searching address (TOC data stored in external RAM). However, when X is also designated as the searching value with the searching address unclear (e.g. TOC data not read out), stage 9 (256 tracks) is set.

Time difference	Set stage (number of tracks)
6 ~ 10 sec	Stage 5 or 6 (15 or 31 tracks) ....Dependent on the present pickup position.
Less than 6 sec	Stage 5 (15 tracks)
Searching address unclear	Stage 9 (256 tracks)

Table 3-1E Set stage and time difference

[2] When the searching position is outside the present position, forward kick operation in which the pickup is moved by the number of tracks corresponding to the stage No. is performed. When the searching position is inside, backward kick operation in which the pickup is moved by the number of tracks corresponding to the stage No. is performed.

[3] After completion of kick operation, the present address data is read out.

[4] Judges whether or not the pickup crosses the searching position. If it does not cross, step [2] is performed again. If it crosses, step [5] is executed. For example, when the address before kick operation is TNO = 12, X = 02 with the searching data of TNO = 12, X = 03, forward kick operation is performed. After completion of kick operation, when the address is of TNO = 12, X = 02 step [2] is executed again, while when TNO = 12, X = 04, step [5] is entered.

3. OPERATION OF MAIN MICROPROCESSOR

In addition, concerning the set number of tracks, as the stage No. lowers by 1, the number of tracks becomes nearly half. Therefore, normally, the pickup crosses the searching position by around 2 or 3 kick operations with the same stage. However, the pickup is moved back a lot if vibration or disc flaw exist. In this case, more than 3 kick operations with the same stage are needed to cross the searching position. In DP-1100B/II, when more than 10 kick operations with the same stage are performed, a measure to raise the stage No. by 1 (the number of tracks is nearly doubled) is taken to shorten the search time.

[5] Process advances to step [6] or [7] according to whether or not backward 1-track kick operation is made.

[6] The stage No. is lowered by 1 to reverse the kick direction. However, as shown in Table 3-1D, if the last pickup movement was the forward 1-track kick, backward 1-track kick operation is further made until the pickup crosses the searching position.

[7] As it is backward 1-track kick operation, the present position is 1 track (0.12 to 0.33 sec) ahead from the target position. Thus, it waits in play mode (muting ON.....Code 3) until the pickup goes across the searching address. When the pickup crosses the address, the designated play/pause mode is engaged, then a series of search operation is complete.

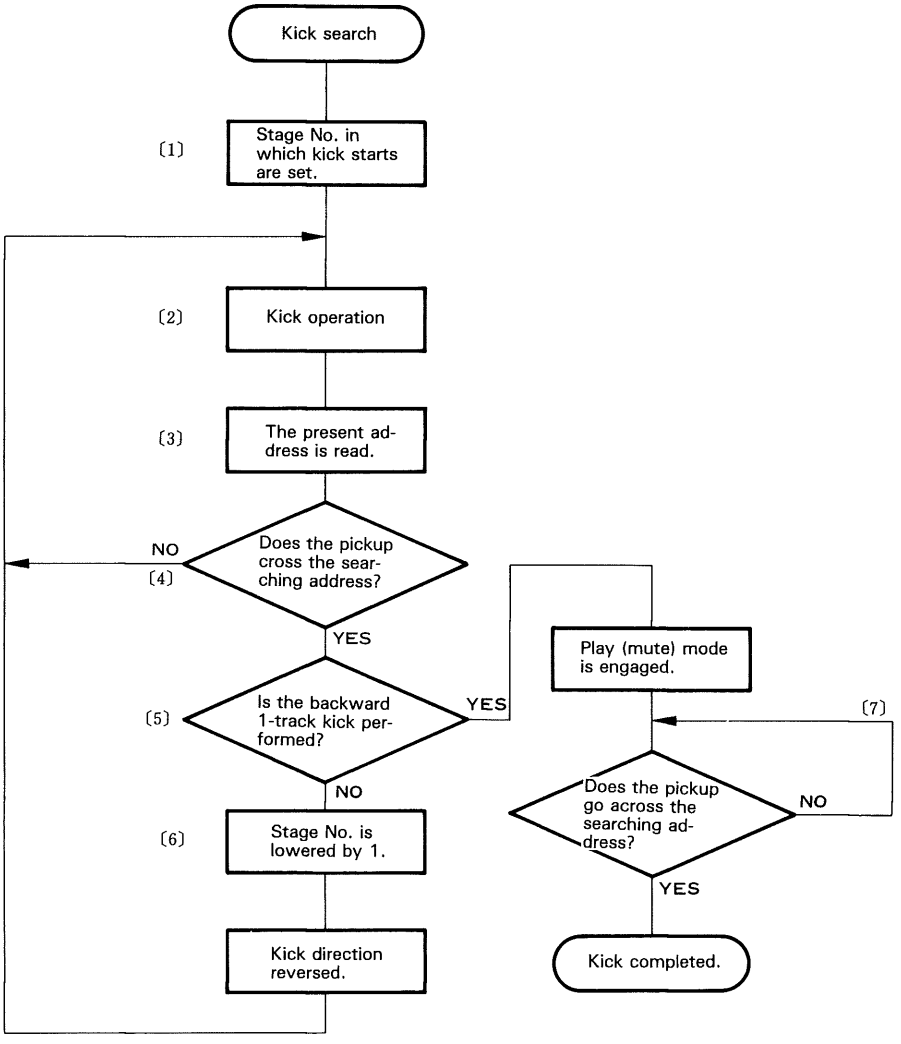


Fig. 3-1H Operation flow chart of kick search system

3. OPERATION OF MAIN MICROPROCESSOR

3-1-8 Pause operation

The pause operation is performed by application of the search system described in section 3-1-7 ''Search operation''.
The following is the operation procedure.

(1) The absolute time (min, sec and ten's digit of frame value) at the point of time when the PAUSE key is pressed is stored in memory as the searching address.
In DP-1100/B, the ten's digit of frame value is also stored in the memory to improve precision in pause operation.

(2) The stage No. in which kick starts is set to stage 2 (backward 3-track kick), upon which search operation is then started.

(3) Even when search is converted, kick in the direction of the disc center is performed to continue search operation.

(4) When the key operation to cancel pause mode is performed, the pause operation (search operation) is completed after convergence of search.

In addition, when the key operation to cancel pause mode is not performed even after lapse of approx. 1 hour after start of pause operation, the protective function works to enter the stop mode automatically to turn OFF laser diodes.

3. OPERATION OF MAIN MICROPROCESSOR

3-2 DATA TRANSMISSION RECEPTION BETWEEN IC15 (TMP4740N : MAIN CPU) AND IC1 (TMP47C41N : DISPLAY MICROPROCESSOR)

a. Data transmission from IC15 (TMP4740N) to IC1 (TMP47C41N)

1. Pin DAT21 is made "H". (IC15 (TMP4740N))
2. Pin DAT21 is checked in periods of 4 msec. If it is "H", reception processing starts. 4 bits of transfer clock pulses are generated. Thereby, 4-bit data is received from IC15 (TMP4740N). (IC1 (TMP47C41N))
3. IC15 (TMP4740N) makes the next transmission data ready. IC1 (TMP4741N) outputs transfer clock pulses (SCK) until the data is completely transmitted.
4. After transmission of the transmission completion data, pin DAT21 is returned to "L" and transmission is completed.

b. Data transmission from IC1 (TMP47C41N) to IC15 (TMP4740N)

1. The data to be transmitted is prepared. (IC1 (TMP47C41N))
2. Pin IRQ is made "L". (IC1 (TMP47C41N))
3. 4 bits of transfer clock pulses (SCK) are output. (IC15 (TMP4740N))
4. 4-bit data is received. (IC15 (TMP4740N))
5. For reception of the next word, step 3 is executed. (IC15 (TMP4740N))
6. The second 4-bit data is received. (IC15 (TMP4740N))
7. Output pin IRQ to IC1 (TMP47C41N) is made "L". Thereby, communication mode is changed to the transmission from IC15 (TMP4740N) to IC1 (TMP4741N).
   This is normal mode.

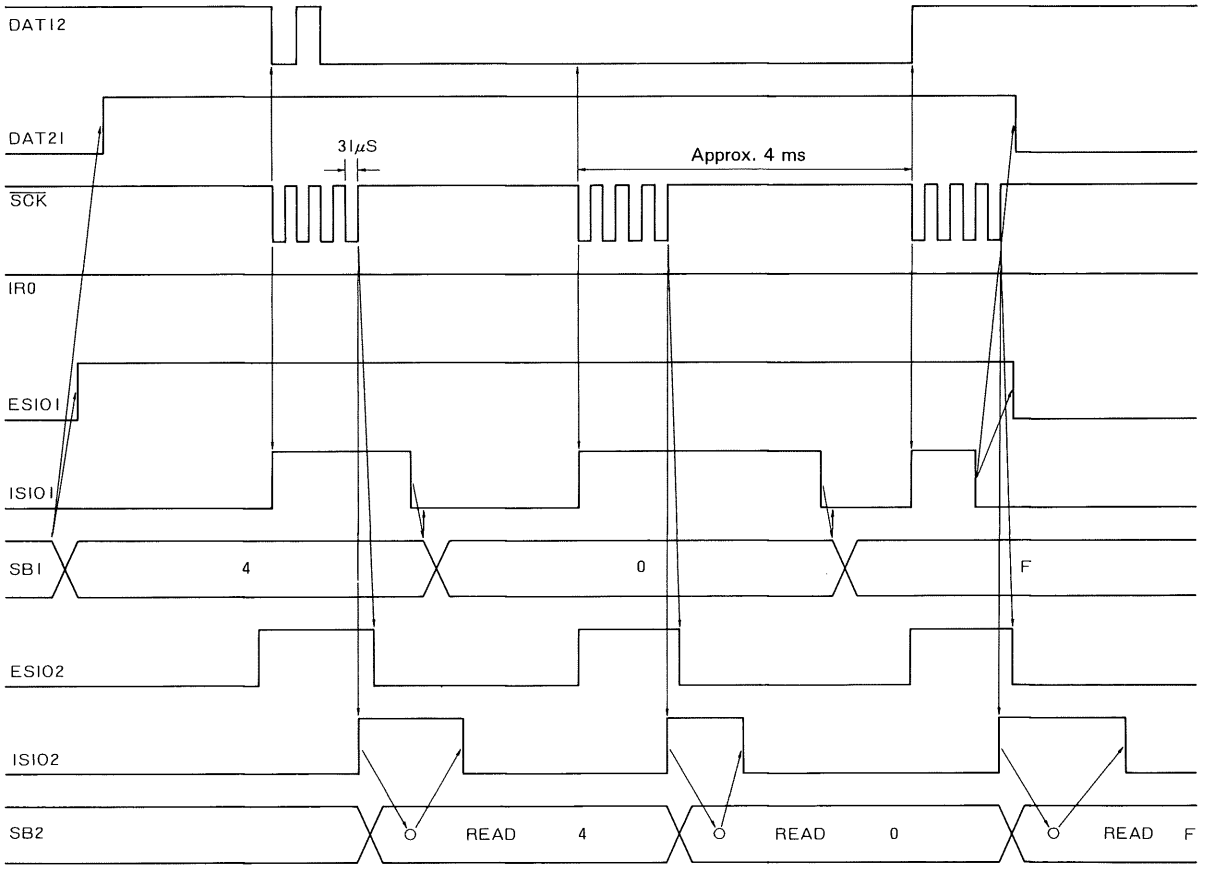


Fig. 3-2A Operation timing diagram of data transmission from IC15 (TMP4740N) to IC1 (TMP47C41N)

4. TROUBLESHOOTING

4-1 Checking flow chart of the start operation from the moment power is switched on until operation is enabled. *Actual action taken by DP-1100B/II

Circuits and signal line written in parenthesis in the left column is the place to be checked.

POWER ON

The microprocessor is reset.
(reset circuit)

The tray position is detected.
(limit switch): SLT
(close or open): CLS, OPEN
*When it is open, the tray is retracted and proceed to the next operation.

The pickup position is detected.
(limit switch)
(SLT)
(P.U. motor circuit)
*When the pickup is at the outer tracks of the disc, it moves to the innermost tracking position and proceed to the next operation.

Laser diode goes on; focus search starts; forward kick; the disc motor operates instantaneously.
(LDC, focus search (FSRCH), PUFB, FGS, inverter buffer output MSP)
(kick motor circuit)
*When there is no disc, the motor rotates in the forward direction momentarily (clockwise), then in reverse (approx. 2 sec.).

Absence or presence of the disc is detected.
(Focus error, DOK)
(Focus servo)
*When there is no disc, the laser diode goes out, then focus search stops and fluorescent indication "DISC" goes out.

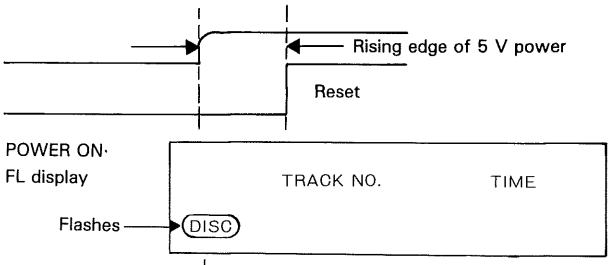
DISC motor start
(IC15, MSP, AFC, CLV)

RFOK is detected.
(S1, S2, EFM, RFOK)
(Focus servo, AGC)
(Slice level)

Focus servo on
Focus search stop
(FOK)
*T max. is detected.
(Focus servo)

Tracking servo on
(FOKG, KGC, TE: Tracking error)
(Tracking servo) (Dropout control)

Ⓐ



Pull out the tray, then switch on the power without inserting the disc.

The tray is retracted.

The pickup moves slightly backwards, and the laser diode is reflected in pale red on the pickup lens.
The pickup moves 1 mm or so vertically.

The disc motor momentarily rotates in the forward direction, then reverses for about 2 sec. before stopping. The fluorescent display DISC goes out.

Pull out the tray, then insert the disc.

The tray is closed.

The disc rotates momentarily, then resumes normal revolution.
(If it does not rotate, check DOK, and AFC.)

With the sound of the rotating disk, the EFM presents jitterless waveform. (FOCUS, tracking servo on)
*If there is no sound and the EFM, RFOK, or EFM waveform is jittered, check the tracking circuit.

Ⓑ

4. TROUBLESHOOTING

Ⓐ

Microprocessor for error setting operates.

(A, B, C, INH)
(IC12)
(CLV bit sync)

* The EFM waveform distorts, then resumes. Upon completion of the operation, fluorescent indication ┌DATA┐ flashes.

Kicked to the TOC position.

(PUFB)
(P.U. feed motor circuit)
(Kick circuit)

* After backward kick is applied, the forward kick is performed. (for brakes)

TOC is read.

(Q data, memory R/W, QDRD, QDRE, Signal processing, main microprocessor)

The pickup is kicked to the beginning of the first program.

(kick circuit)

Pause at the beginning of the first program

The fluorescent display shows:

	Track No.	Time
┌DATA┐	01 01	00 : 00

Is indication normal?

(Display circuit)

Press the PLAY button.

Is sound heard? Is it free from abnormal sound?

(Signal processing, DAC)

Is there sound skipping?

(Tracking servo, dropout control)

Is the time indication advanced?

(Display circuit, main microprocessor)

Press the PAUSE button.

Is the sound muted?

(Signal processing, DAC, IC19)

Is the time indication stopped at a certain reading?

(Kick circuit)

Press the PLAY button.

Ⓑ

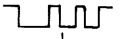
The EFM waveform is distorted, then resumes normally.

The fluorescent display ┌DATA┐ flashes (SVC setting is complete).

The pickup moves frontwards.

The signal appears at QDRD, Q data, memory R/W.
(Reading to TOC is complete.)

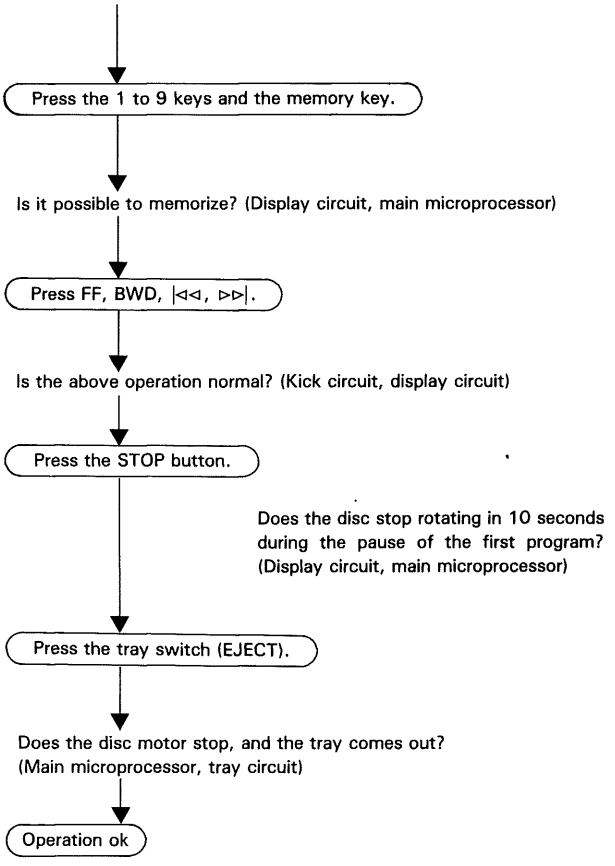
The pickup moves backwards. (The RFG waveform will be as shown.)



(The pickup is set to the position of the beginning of the first program.)

Pause at the beginning of the first program

4. TROUBLESHOOTING



4. TROUBLESHOOTING

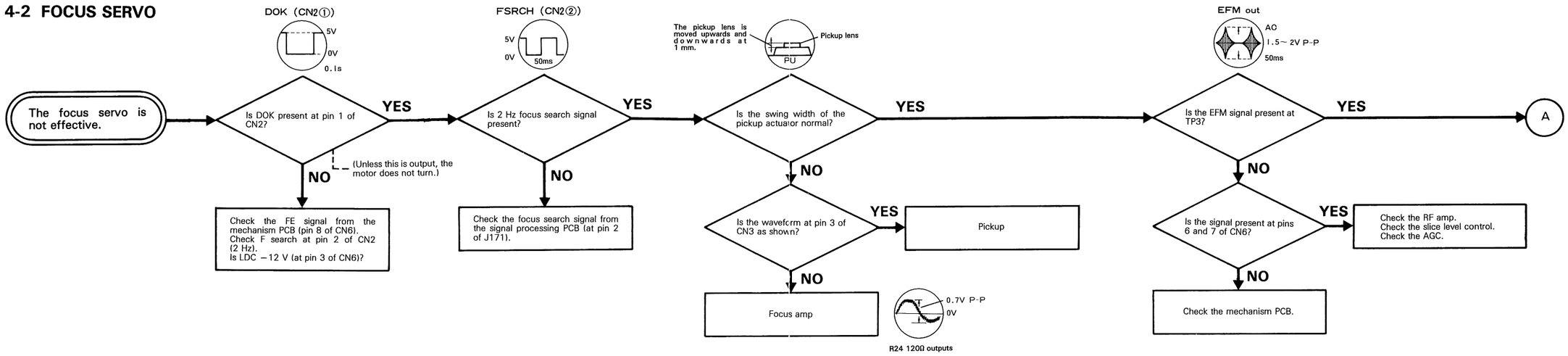
4-1-1 Functions of respective display divisions

Indicator	Main functions
DATA	When TOC data is all read out normally, lights after completion of search for first program. In addition, it blinks while TOC data is read out.
DISC	After the OPEN/CLOSE key is pressed, blinks during tray open/close operation. In addition, it lights only when the disc is loaded correctly with the tray closed.
PAUSE	Lights in pause mode. When the PAUSE key is pressed as a substitute for the OPEN/CLOSE key, it blinks until search for the first program completes. It also blinks when the pickup is carried to one of both ends of the program area by FF or REV operation.
PLAY (PLAY INDICATOR)	Lights in play mode. In addition, when the PLAY key is pressed as a substitute for the OPEN/CLOSE key, it blinks until search for the first program is completed.
M-PLAY	Lights in memory play mode.
M-SCAN	Lights when the M-SCAN function is ON.
TOTAL-TIME	Lights when the time display mode is the absolute time mode. (+TOTAL)
REMAINING-TIME	Lights when the time display mode is the remaining time mode. (−REMAINING)
REPEAT	Lights when the repeat function is ON.
MEMORY CHANNEL	In manual play mode, those lamps corresponding to all memory channels written light. In addition, in memory play mode, only those lamps corresponding to all playable channels light. However, when all channels are not playable, all lamps blink.
MEMORY	In memory play mode, those lamps corresponding to those memory channels which are in play at present light. In addition, when a memory channel is read out by operation of the M-READ key, that lamp corresponding to the channel being read out blinks. Then, when data is written in a memory channel by operation of the MEMORY key, its corresponding lamp blinks for 3 sec. after the MEMORY key is pressed.

Table 4-1A

4. TROUBLESHOOTING

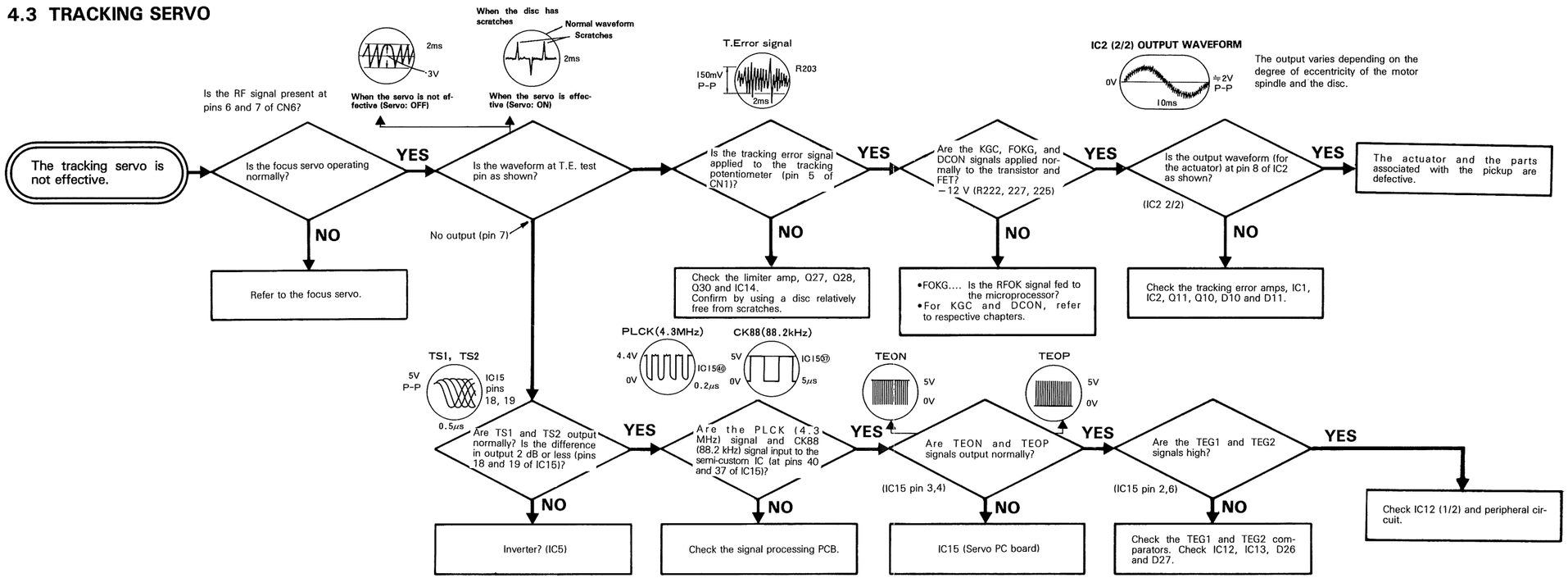
4-2 FOCUS SERVO



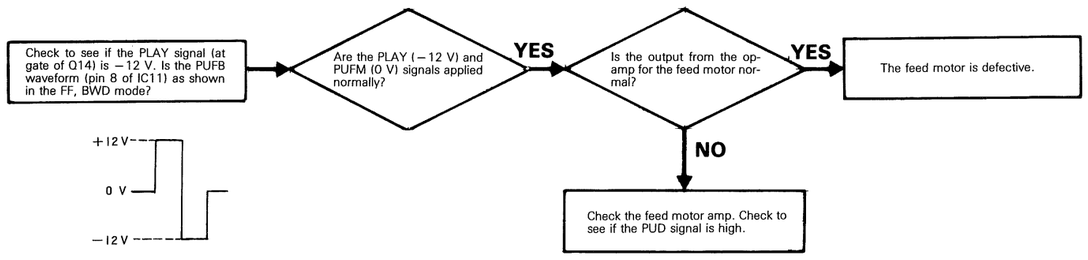
* The pickup position should be at inner tracks.

4. TROUBLESHOOTING

4.3 TRACKING SERVO

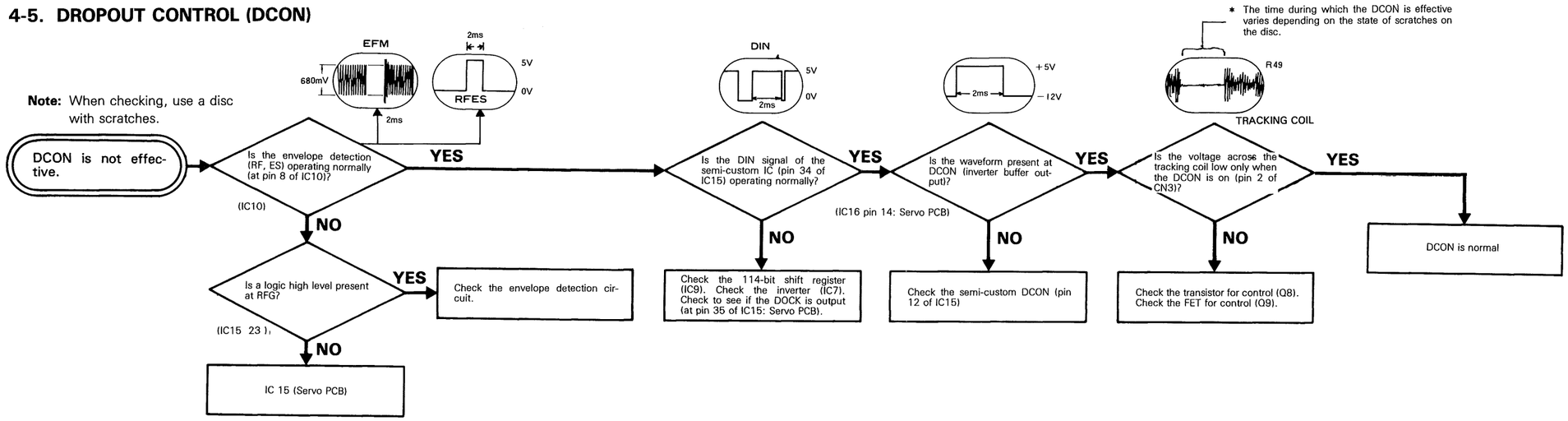


4-4. Pickup feed motor circuit

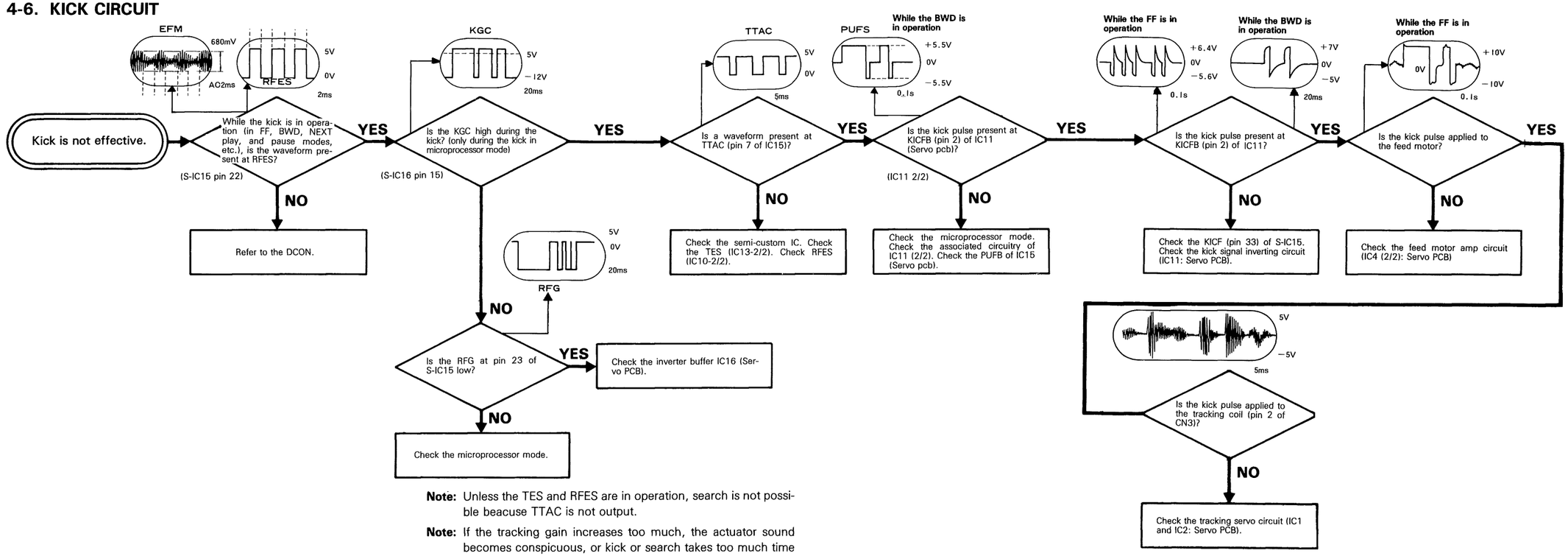


4. TROUBLESHOOTING

4-5. DROPOUT CONTROL (DCON)



4-6. KICK CIRCUIT

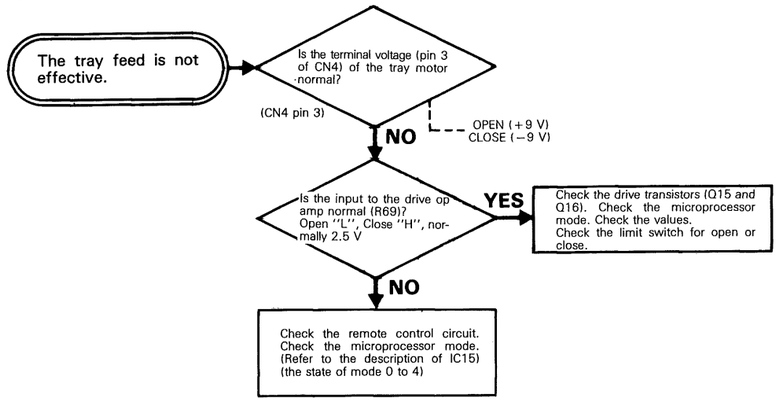


Note: Unless the TES and RFES are in operation, search is not possible beacuse TTAC is not output.

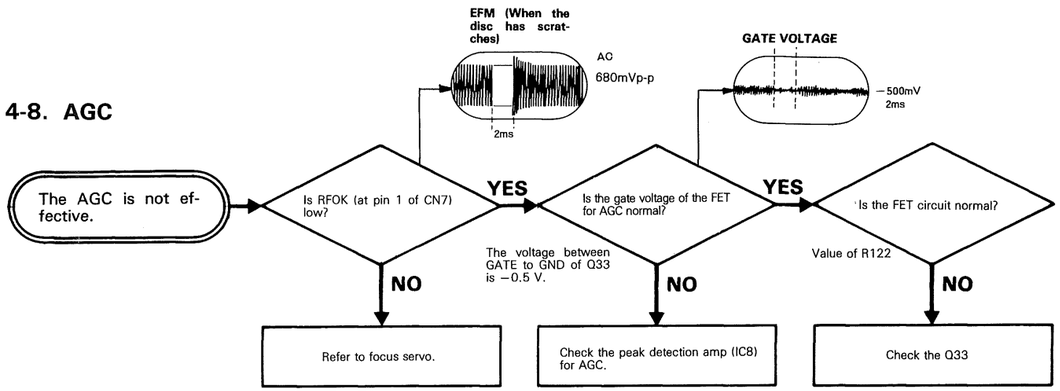
Note: If the tracking gain increases too much, the actuator sound becomes conspicuous, or kick or search takes too much time or even worse, programs cannot be read. Therefore, in case of doubt, check the gain.

4. TROUBLESHOOTING

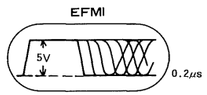
4-7. TRAY

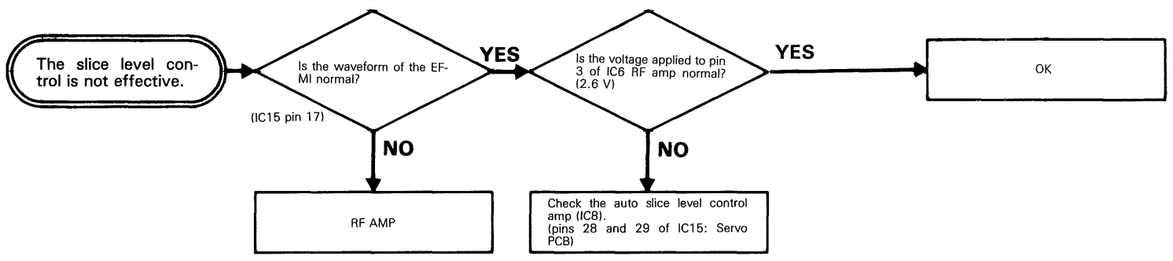


4-8. AGC



4-9. SLICE LEVEL CONTROL (D.S.V)



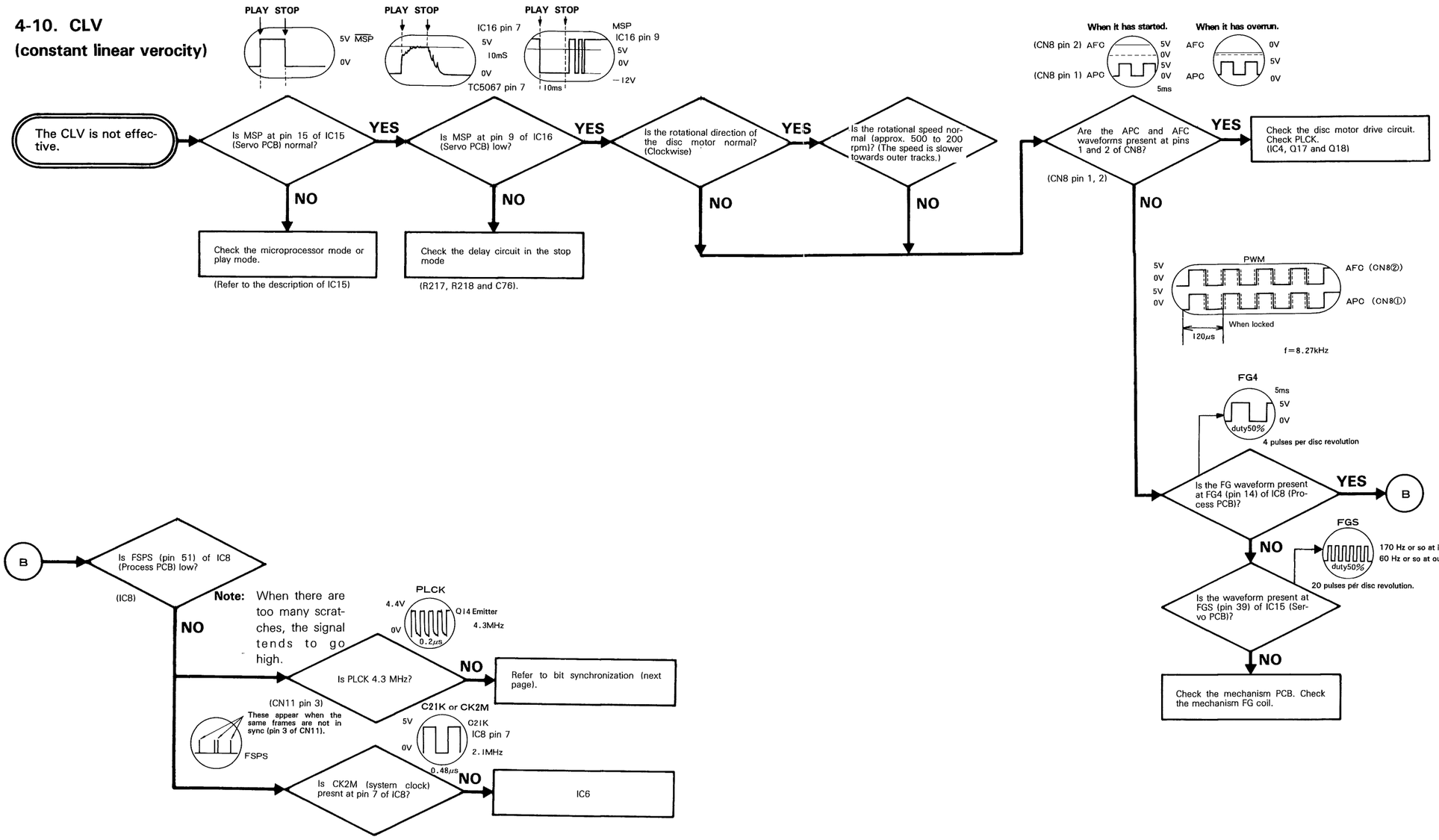


Note: The AGC circuit makes the input level to the RF amp constant when the input level has changed due to the variation in disc speed or scratches on the disc.

Note: The slice level control circuit eliminates the DC component in the EFM wave.

4. TROUBLESHOOTING

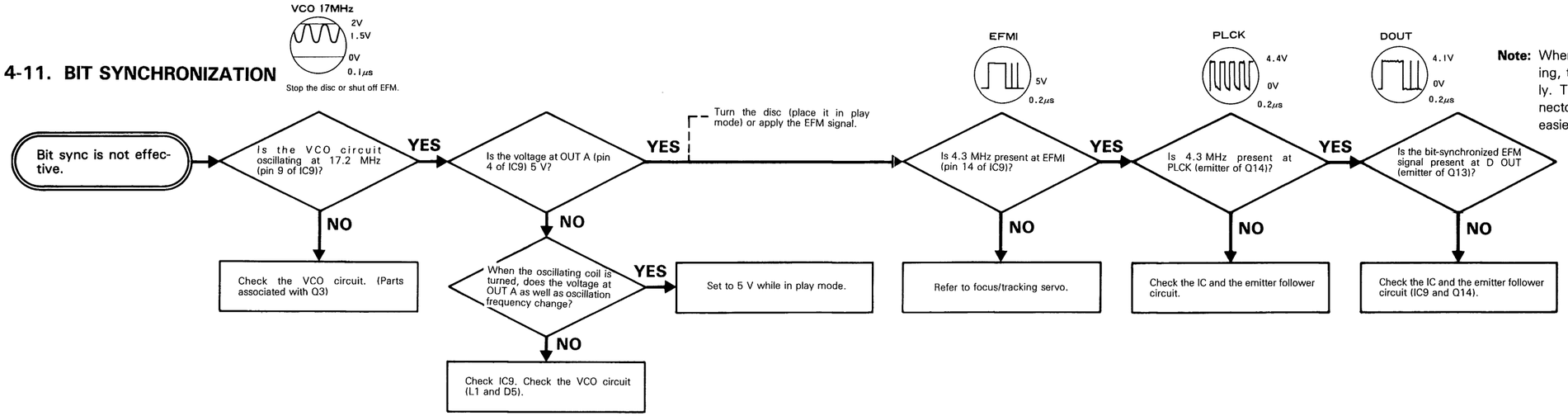
4-10. CLV
(constant linear verocity)



Note: When the pickup is outside the disc, the disc rotates at high speed. The same is true when PLCK is not present at IC15 (Servo PCB) or when −12 V is not present.

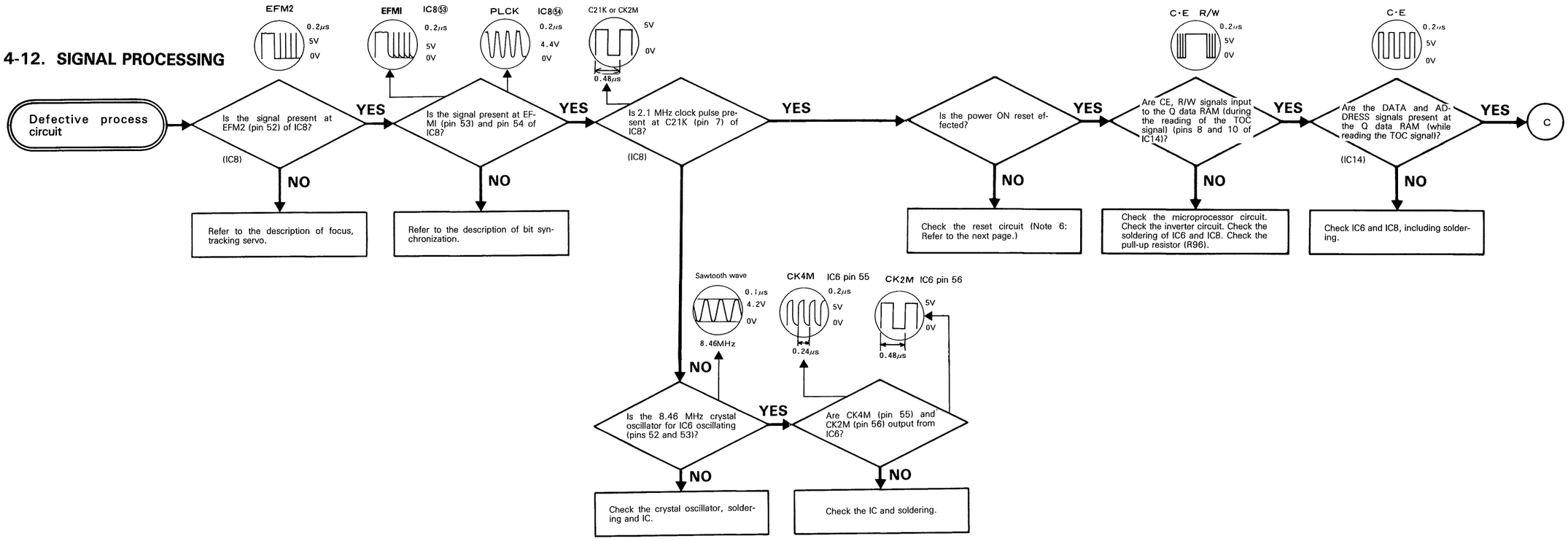
4. TROUBLESHOOTING

4-11. BIT SYNCHRONIZATION

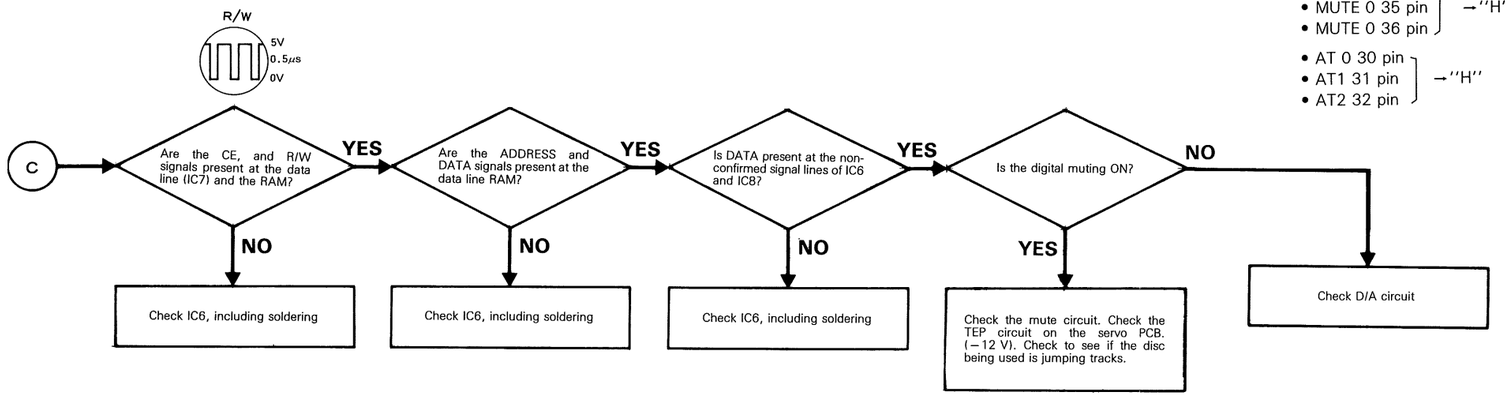


Note: When the microprocessor is malfunctioning, the symptom does not appear clearly. Therefore, disconnect the SVC connector (CN10), then operate manually for easier confirmation of the symptom.

4-12. SIGNAL PROCESSING



4. TROUBLESHOOTING



State where muting is not effective.

- TEP→ ''−12 V''
- MUTE 1 34 pin
- MUTE 0 35 pin
- MUTE 0 36 pin

→''H''

- AT 0 30 pin
- AT1 31 pin
- AT2 32 pin

→''H''

Note: **1.** The level at the signal processing digital line is either 0 V or 5 V. Therefore, the values in between never appear. If such values should appear, check the PCB pattern for bridge soldering or broken pattern.

2. Since EFM2 contains a lot of jitter, the rising and falling edges are blurred.

3. Easy way to find the bad soldering of the flat IC leads is to check the signal at patterns for output ports and check the signal at pins for input ports.

4. Easy way to find the bad soldering of flat IC leads is to use an awl or equivalent tool as shown in the figure below.

5. The PLCK and EFM1 signals should be PLL-locked.

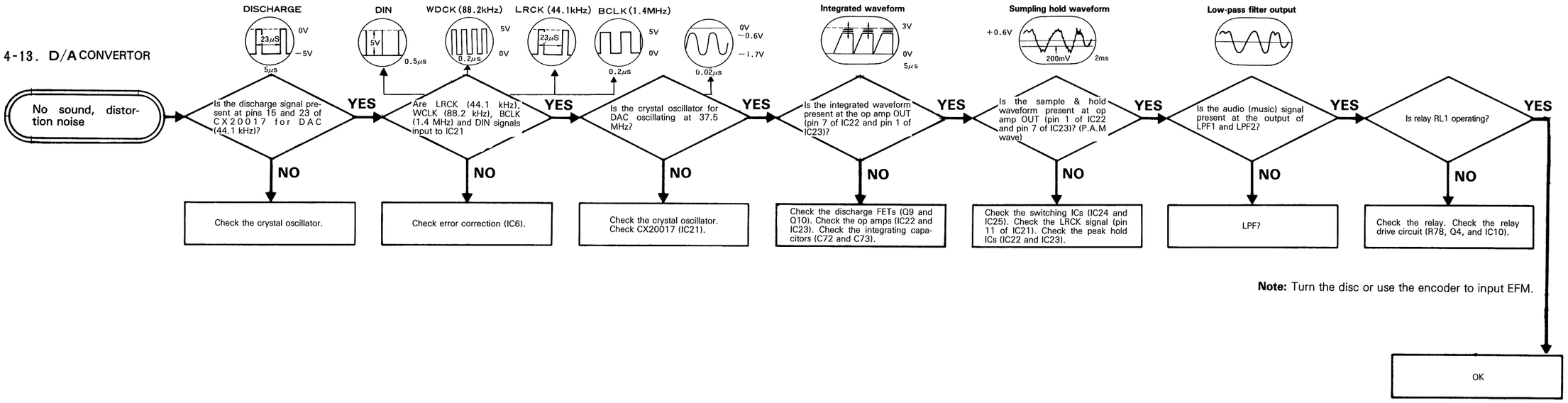
6. Checking method of the power ON reset

- Pull out the tray, then set the disc.
- Turn on the power switch.
- The tray is retracted, then the disc starts rotating.
- The fluoresent display: (DISK) blinks, and TRACK NO. and TIME light.
- The EFM waveform which is free from jitter, etc. appears once, then it is distorted.

If the foregoing applies, the power ON reset is regarded as acceptable.

7. PAM: Pulse Amplitude Modulation

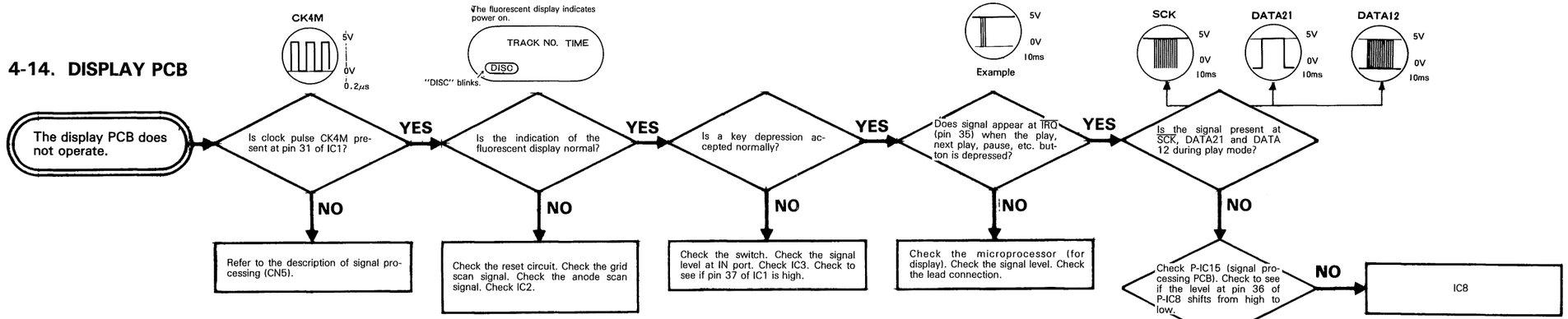
4-13. D/A CONVERTOR



Note: Turn the disc or use the encoder to input EFM.

4. TROUBLESHOOTING

4-14. DISPLAY PCB



* When read-in has completed,

Remote control "H"

Tray "H"

RESET "H"

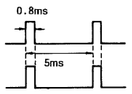
IRQ "H" (A pulse is output only when the play, pause, etc. button is depressed.)

DATA12 "H"

SCK "H" Signal is output only during play mode.

DATA21 "L"

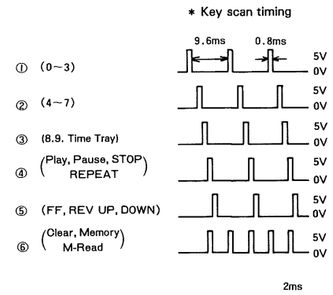
Timing of the latch for lighting the LED



0.5 msec. clock pulse

5 msec.: Play and pause, anode scan signal

* Key scan timing



5. MECHANISM OPERATION

5-1 BRIEF DESCRIPTION OF MECHANISM SECTION (Details described later in each chapter)

5-1-1 Pickup slide mechanism

(1) Operation

Two worm gears and one wheel gear are rotated by the pickup carry motor. This rotation is transmitted to the rack gear by which the pickup in turn performs a linear motion.

(2) Construction

The worm gear in the carry motor is engaged with the wheel gear. Thus, another worm gear attached to the drive shaft connected to the wheel gear are engaged with the rack gear.

5-1-2 Eject and loading mechanism

(1) Operation during power ON

In this unit, the eject and loading operations are the complete reverse to each other.

a) When the OPEN/CLOSE button is pressed with the tray closed, the loading motor rotates and the loading gears do so also. Thus, as the tray goes out forwards by motion of the two tray racks, the metal at the rear of the tray rail strikes the opened tray detection leaf switch so that the loading motor stops.
Then, the eject operation is complete.

b) When the OPEN/CLOSE button is pressed with the tray open, the tray drive rack is driven by the loading gears. Thus, when the tray reaches the position at which it is housed, it is released from the drive rack. At this time, the tray clamp rack begins to move. The tray thereby is lowered rotating and at the same time the clamper lever also lowers. Then, when the clamper clamps the disc to the disc turntable, the clamper gear strikes the closed tray detection leaf switch so that the loading motor is stopped by the microprocessor. The loading operation is then complete.

c) The eject operation is controlled by the microprocessor to stop the disc rotation completely to avoid damage of the disc before the tray is sent out. Therefore, a slight time lag exists from the time OPEN/CLOSE button had been pressed.

(2) During power OFF

In this case, the tray does not move even if the OPEN/CLOSE button is pressed. When the tray is to be ejected without power ON for repair, remove the top case and rotate the clamper gear manually. When the tray moves around 5 mm by full rotation of the clamper gear, it can be opened when pulled outward manually.

5-1-3 Tray section mechanism

(1) Tray operation

a) When the clamp rack is pulled rearwards, the link shaft put in the clamp rack presses the link to rotate disc tray B (disc shaped section).

b) Disc tray A (square molded section) has cam grooves inside. As a catch of disc tray B is engaged with a cam groove, disc tray B descends rotating along the cam groove section.

(2) Tray grounding mechanism

This mechanism prevents faulty operation of the unit due to the static electricity (several kV to tens of kV) charged in the human body when the OPEN/CLOSE button is pressed with the tray open.

5-1-4 FG mechanism

The FG mechanism is provided to produce a signal to detect the disc rotating speed. FG magnets are magnetically attached to the disc motor shaft alternately in respect to N and S poles. When these magnets rotate, an electromotive force appears in the FG PCB vicinity. This force is taken as a FG signal.

5-1-5 Start limit switch

When the OPEN/CLOSE button is pressed, the pickup carry motor rotates to move the pickup to the beginning of the first program wherever the pickup is positioned. The start limit switch detects the beginning of the first program.

5-1-6 Head amplifier PCB section

The head amplifier PCB section performs the following three functions:

a) It handles the light reception signal from the 4-division photodiode detector in the pickup to generate the focus error (FE) signal and signals S1 and S2 from which the tracking error (TE) is produced.

b) It controls the laser output.

c) It amplifies the FG signal and converts it to a pulse signal.

5. MECHANISM OPERATION

5-2 MECHANISMS AND THEIR OPERATIONS

5-2-1 Pickup slide mechanism

(1) Operation (See Fig. M1.)

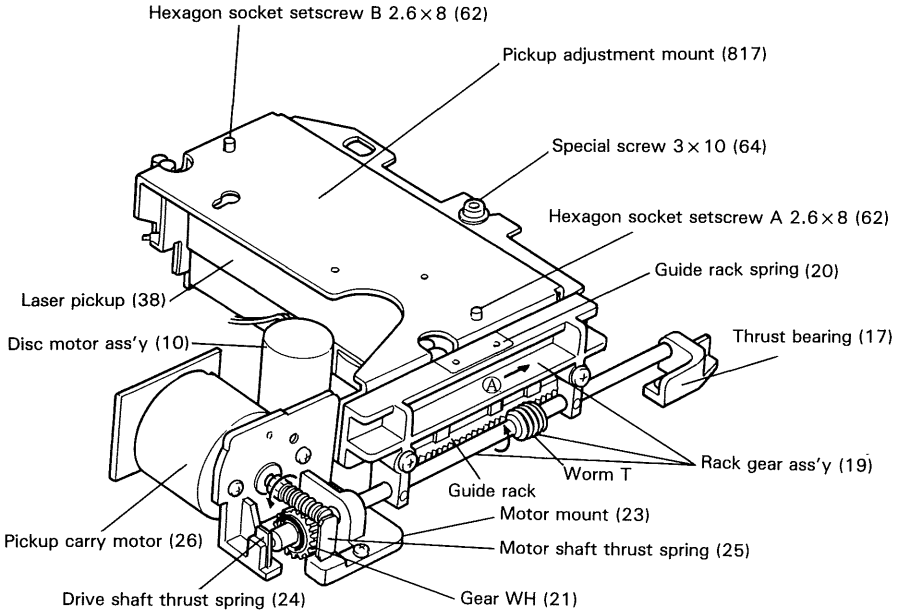


Fig. M1 Laser pickup slide mechanism

Explanation is given only for forward mode (during play or when the pickup is fast forwarded). The direction of each arrow used is reverse in reverse mode.

a) When carry motor (26) rotates, the plastic worm gear of motor turns in the direction of the arrow.
b) Gear WH (21) is driven by engagement with the worm gear.
c) Gear WH (21) has the drive shaft jointed by D-shape engagement. Worm T attached to the drive shaft also turns in the direction of the arrow together with gear WH (21).
d) The guide rack moves by engagement with worm T.
e) Pickup adjustment mount (817) and laser pickup (38) secured to the guide rack perform linear movement in the direction of arrow (A).

(2) Construction

a) The drive shaft, worm T and the guide rack, which are unified, are service parts as gear ass'y (19). Worm T is attached with adhesive to the predetermined position.
b) The carry motor and the plastic worm gear, which are unified by force fitting, are service parts as motor ass'y (26).
c) Motor shaft thrust spring (25) and drive shaft thrust spring (24) exert force on the motor shaft and the drive shaft in the direction of thrust to eliminate the servo lag time due to inconstant thrust when the pickup is driven. The function of these springs makes inconstant thrust adjustment unnecessary.
d) Function of guide rack spring (See Fig. M2.)
The guide rack spring enables the pickup to be driven by the worm T and the teeth of the guide rack when the unit (mechanism) not placed level. Normally, with the unit (mechanism) placed level, a gap exists between the guide rack and the guide rack spring. When not placed level, the spring applies enough force to the guide rack so that the engagement of worm T and the guide rack is the same as when placed level.

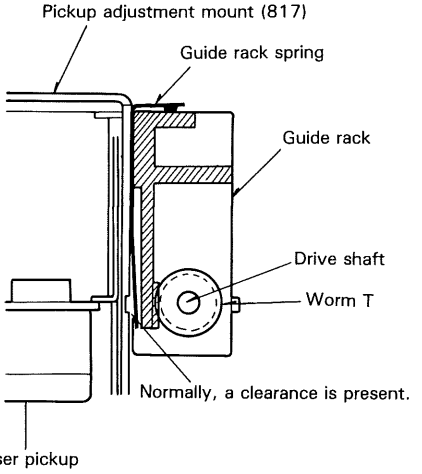


Fig. M2 Function of guide rack spring

5. MECHANISM OPERATION

5-2-2 Eject and loading mechanism

(1) Operation at power ON

Explanation is given only for loading operation from the tray open position. The eject operation is the reverse to the loading operation. In the eject or loading operation, the tray also moves correspondingly. Therefore, also refer to section 5-2-3 ''Tray section mechanism''

a) When OPEN/CLOSE switch S004 is pressed with the tray open (Fig. M3), loading motor (74) rotates in the direction of arrow (A) and loading gears (65) to (69) also rotate. (Fig. M4)

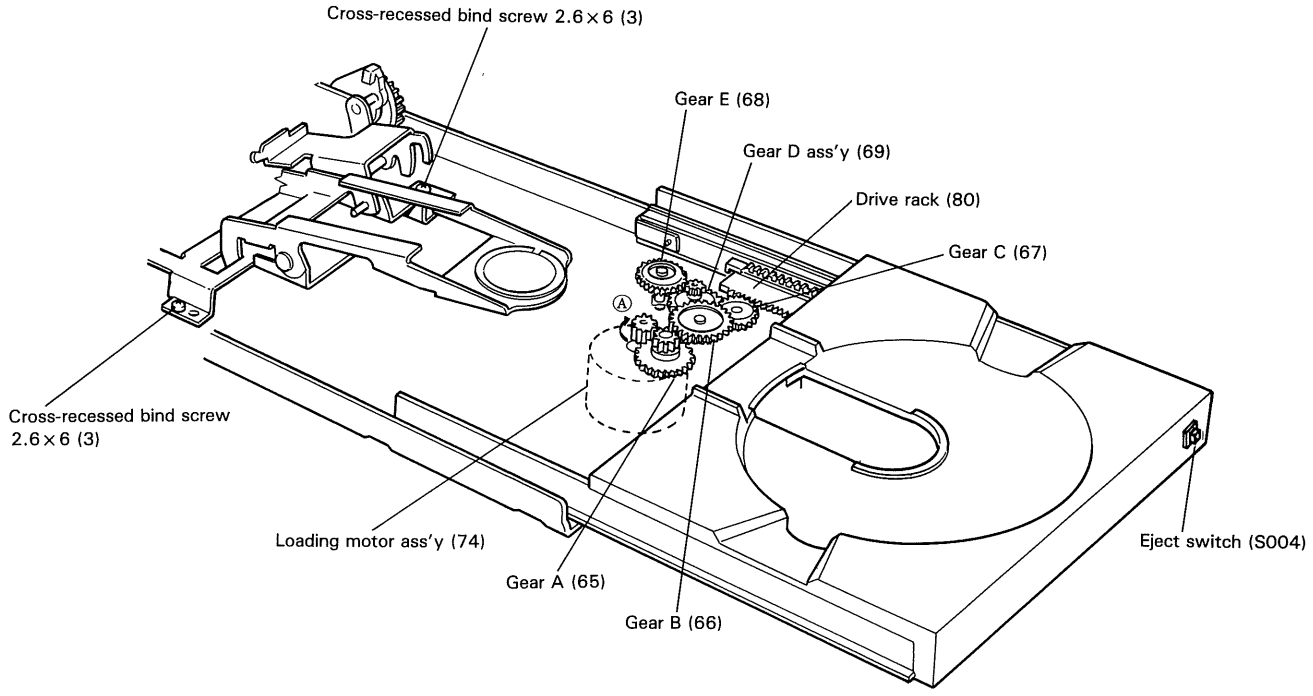


Fig. M3 Loading mechanism

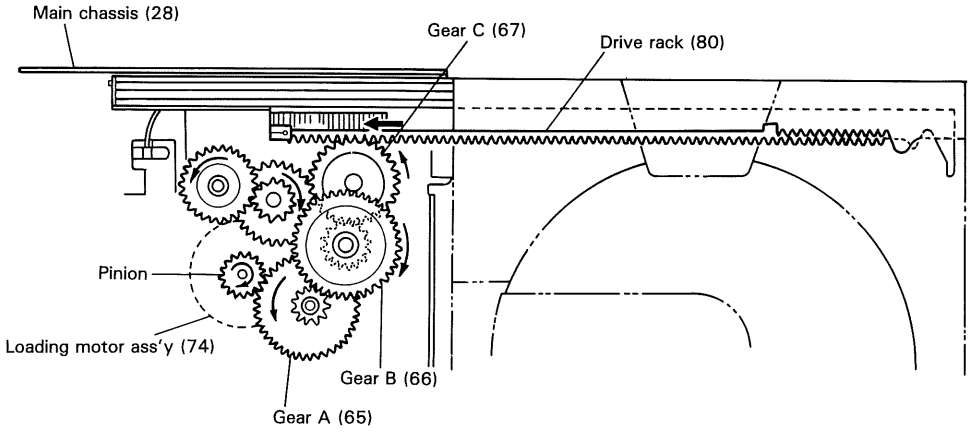


Fig. M4 Loading gear motion and drive rack driving (1)

5. MECHANISM OPERATION

b) Tray drive rack (80) is driven by gear C (67) of the loading gear group so that the tray (ass'y) is retracted into the unit. (Fig. M5)

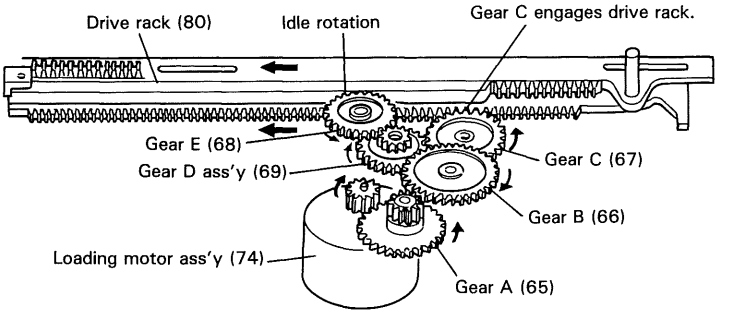


Fig. M5 Loading gear motion and drive rack driving (2)

c) When the tray nears the position at which it is housed, clamper gear (53) starts rotating by means of the upper rack section of clamp rack (82). Clamp rack (82) is pressed in the inside of its long hole by stepped screw (78) to move at the same speed as drive rack (80). (Fig. M6)

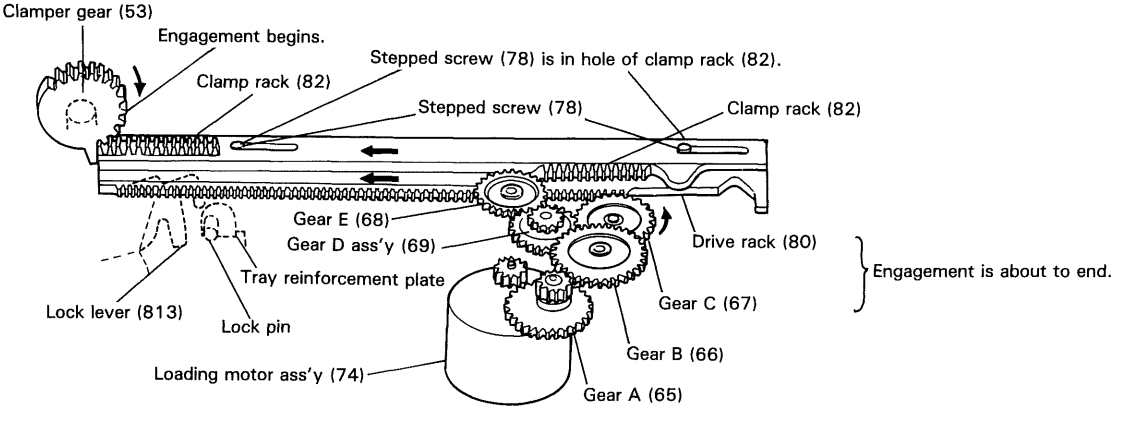


Fig. M6 Relative operation between drive rack and clamp rack (1)

5. MECHANISM OPERATION

d) The tray driven by gear C (67) and drive rack (80) is completed. After that, when loading gear E (68) engages with clamp rack (82), disc tray B (91) (disc shaped section) is lowered also with rotation and clamper gear (53) rotates. Motion of the tray is completed by relay of force from drive rack (80) to clamp rack (82). (Fig. M7)

* For motion of disc tray B, refer to 5-2-3 ''Tray section mechanism''. (Figs. M9, M12 and M13)

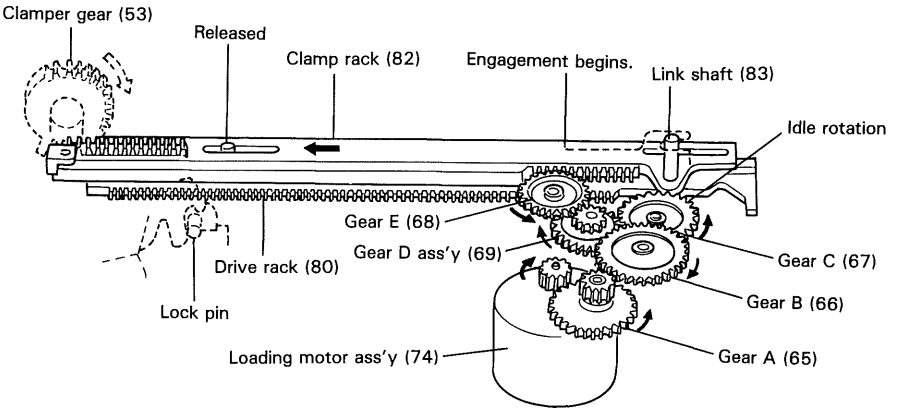


Fig. M7 Relative operation between drive rack and clamp rack (2)

* When operation is relayed from drive rack (80) to clamp rack (82) or when the function of gear D ass'y (69) shifts from step c to d, drive rack (80) completes its own job. Instead, clamp rack (82) takes over the subsequent operation. This relay of operation is made smooth by gear D ass'y (69). (Fig. M8)
In step c, gear C (67), drive rack (80) and clamp rack (82) move at the same circumferential and linear speed. Gear E (68) and gear D (small) have half that circumferential speed, however.
To compensate this, gear D (small) moves earlier than gear D (large) so that gear E (68) can be engaged with clamp rack (82).

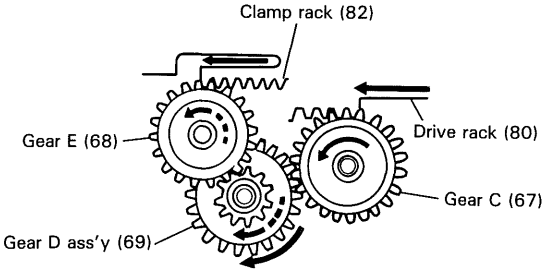


Fig. M8 Operation of gear D ass'y

5. MECHANISM OPERATION

e) Lock lever (813) is moved by the cam section of clamper gear (53). Clamper lever (806) begins to lower correspondingly. (Fig. M9)

f) The clamper section (parts (32), (35), (36) and (37)) mounted on the top of clamper lever (806) also lowers to clamp the disc. The force to clamp the disc is obtained from the attraction power between clamper magnet (36) and the disc turntable made of iron.

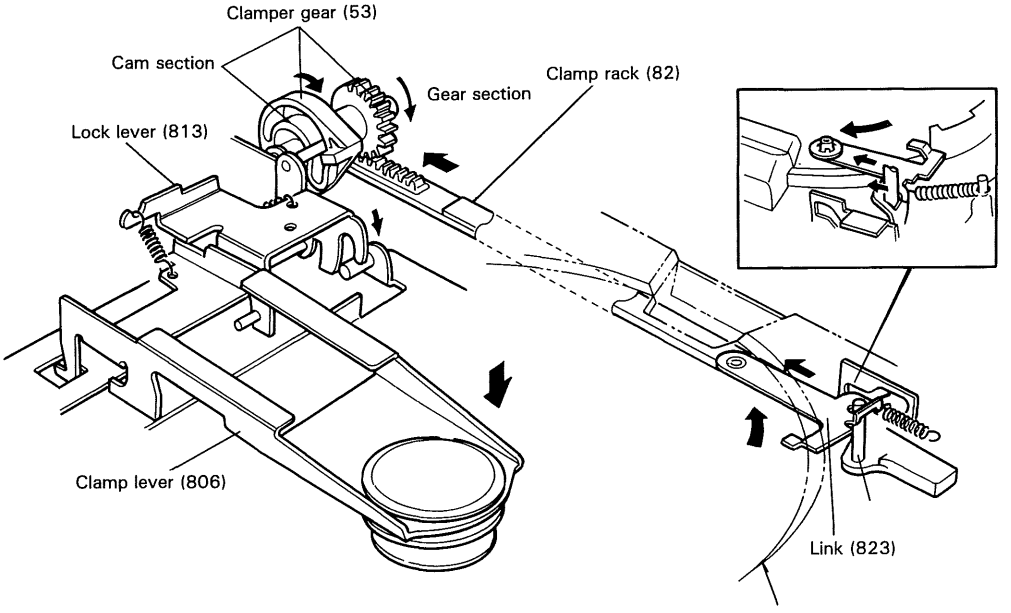


Fig. M9 Tray operation

g) With the disc is clamped, the protrusion of clamper gear (53) pushes the closed tray detection leaf switch attached by screws to clamper lever mounting stand (51) so that the loading motor stops rotation (Fig. M10). Thereupon, the loading operation is complete. Subsequently, the unit implements the following operation:

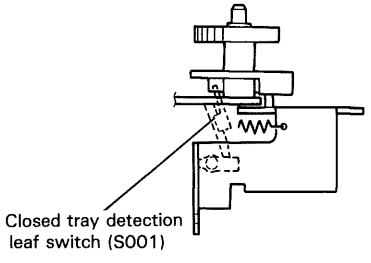


Fig. M10 Closed tray detection leaf switch

h) The microprocessor checks whether or not the disc is present. If present, it rotates disc motor (10) and carries the pickup to the beginning of the first program after reading data TOC. Then, the disc motor is stopped. (When the play button is pressed with the tray open, the disc motor does not stop and play mode is entered as it is.)
If not, the disc motor does not rotate.

Thus, the operation when the OPEN/CLOSE button is pressed from the tray open position is complete. Hereupon, when the OPEN/CLOSE button is pressed again, entirely reverse operation from step (g) to (a) is performed.

(2) During power OFF

When the tray is to be pulled out fully at power OFF, slowly rotate clamper gear (53) (Fig. M9) manually in the direction reverse to that of the arrow until it stops.
When clamper gear (53) has been fully rotated, the tray comes out about 5 mm from the panel surface. Afterwards, the tray can be pulled out frontward by hand.
At this time, when the tray is pulled by an excessive power, drive rack (80) may be disengaged from gear C (67) or rather skips the teeth of the guide rack. However, this case does not mean a failure since the guide rack sways a little away from the gear C to protect the rack and gear from being damaged.
In addition, when the tray is pulled without clamper gear (53) fully rotated, the tray may come out only halfway. In this case, return the tray to the position in which it is housed in.

5. MECHANISM OPERATION

5-2-3 Tray section mechanism

(1) Construction

Disc tray B (91) has a cone-shaped sectional view, as shown in Fig. M11, by which the signal pit surface on the disc is protected against damage. Disc tray B (91) has four catches in its outer circumference. These catches are engaged with the four cam grooves of disc tray A (93) so that the tray section moves up and down concurrently with rotation.

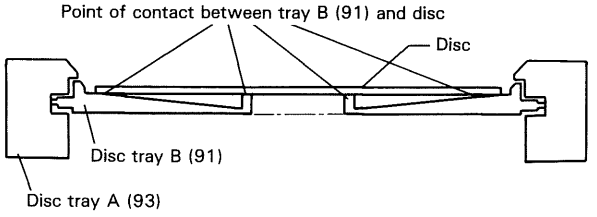


Fig. M11 Construction of tray section

(2) Tray operation

The tray operates as follows when the disc is loaded. The tray operates in reverse when the disc is ejected.

a) Clamp rack (82) is driven by gear E (68). (Fig. M7)
b) When clamp rack (82) moves, link shaft (83) in this rack also moves. (Fig. M9)
c) Link shaft (83) pushes link (823).
d) Disc tray B (91) connected with link (823) begins to rotate.
e) Disc tray B (91) lowers along the cam groove section of disc tray A (93). (Fig. M12)
f) When disc tray B (91) comes to the position shown in Fig. M13, the closed tray detection leaf switch (Fig. M10) works to stop the loading motor, at which time disc tray B (91) also stops. Thereupon, the tray operation is complete. At this time, the pickup is parallel with the notched section of disc tray B (91) in its sliding direction.

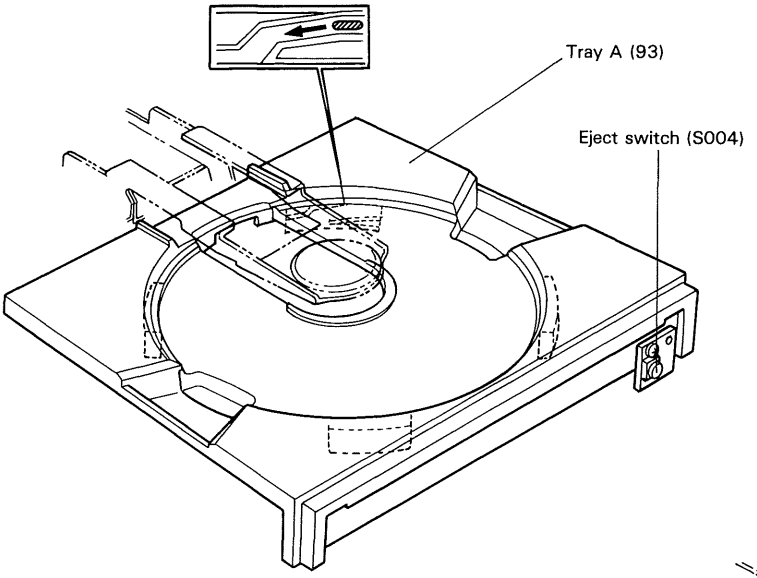


Fig. M12 Tray operation

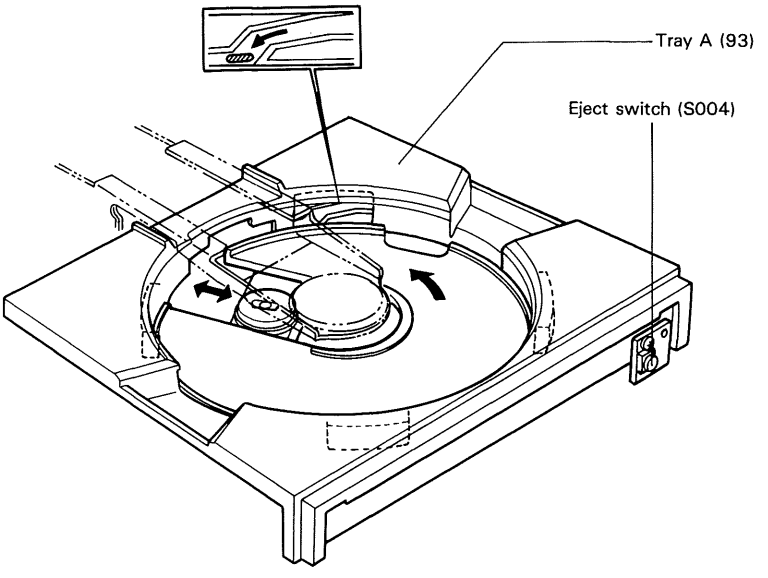


Fig. M13 Tray operation

5. MECHANISM OPERATION

(3) Tray grounding route

The electrostatic charge in the human body may reach a few kV to tens of kV. The electrostatic charge is released via the following route so that the unit is protected from malfunctioning when the OPEN/CLOSE button is pressed with the tray open (Fig. M14).

* In any of those mechanisms of mass-produced products No. 1 to No. 3000, the alumite on the entire bottom side of rail L (822) is scraped off as a substitue method. Thereby, the ground plate spring and the side are brought into contact, thereby grounding the chassis base.

i) Charged finger
↓
ii) Ground pin of OPEN/CLOSE key switch S004
↓
iii) Tray reinforcement plate (821)
↓
iv) Tapping screw 3x8
↓
v) Rail L (822)
↓
vii) Ground plate spring
↓
Viii) Main chassis
↓
ix) Unit enclosure

vi) Ground plate (827) → Viii) Main chassis

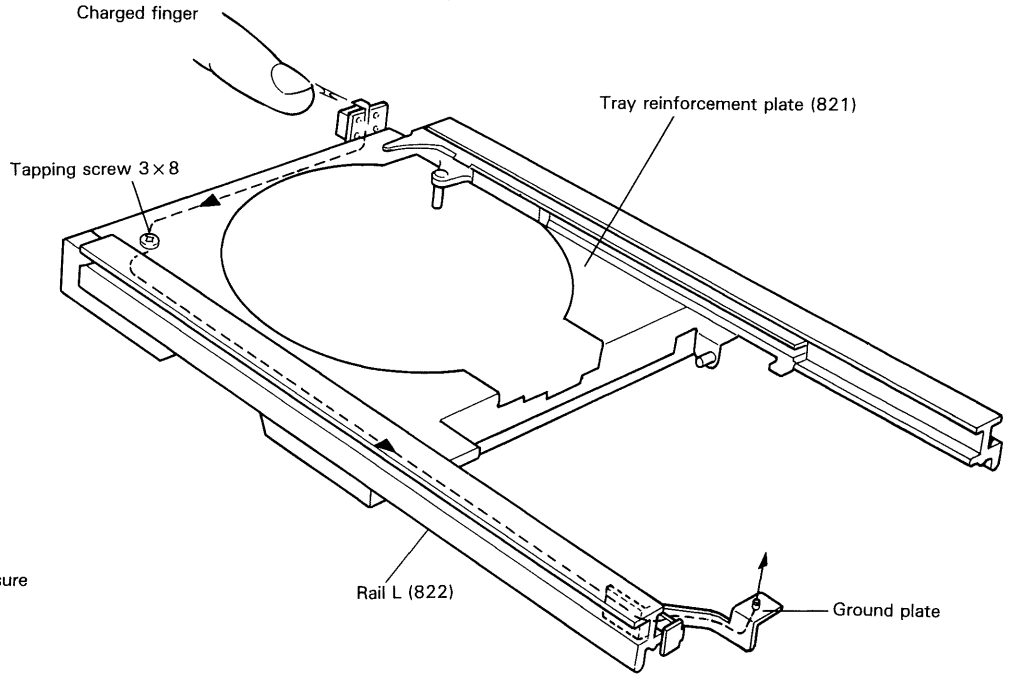


Fig. M14 Disc tray ground mechanism

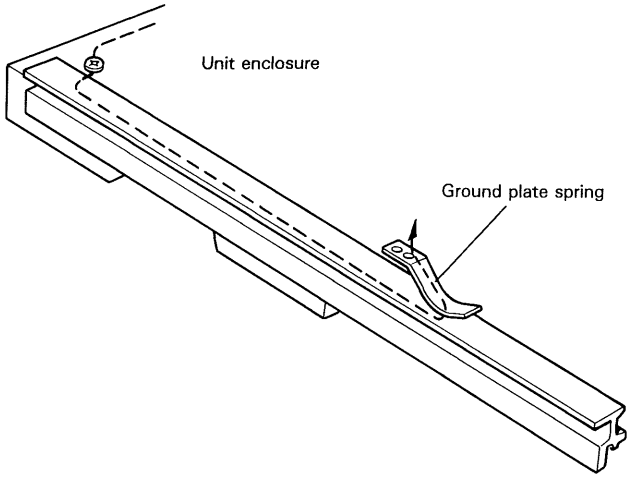


Fig. M15 Disc tray ground mechanism

5. MECHANISM OPERATION

5-2-4 FG mechanism

(1) Construction

a) 20 pairs of N and S pole magnets are radially installed under the disc turntable (Fig. M16). These are unified as motor ass'y (10) for service parts.

b) On the other hand, a PC board with radial and zig-zag circuit patterns is provided, at a slight clearance (0.2 to 0.7 mm) from the above ass'y. (Fig. M17)

c) The relative position between the above two is shown in Fig. M18.

(2) Operation

When the disc motor rotates, an AC electromotive force appears in the FG PCB due to the magnetic field created by the magnet combination. This force is taken as the FG signal to detect the rotating speed of the disc motor.

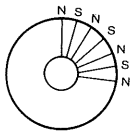


Fig. M16 FG magnet

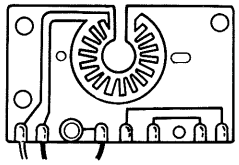


Fig. M17 FG PCB

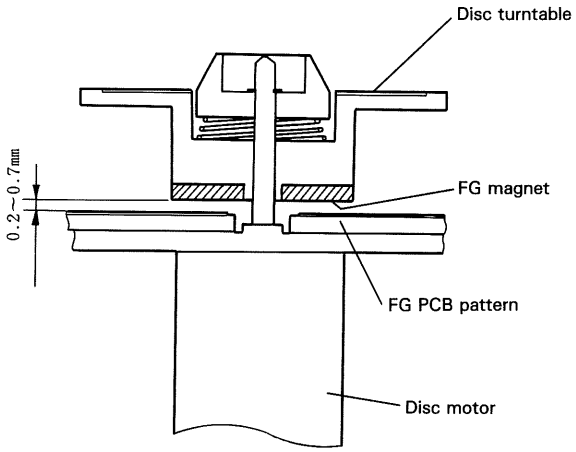


Fig. M18 Disc motor ass'y

5. MECHANISM OPERATION

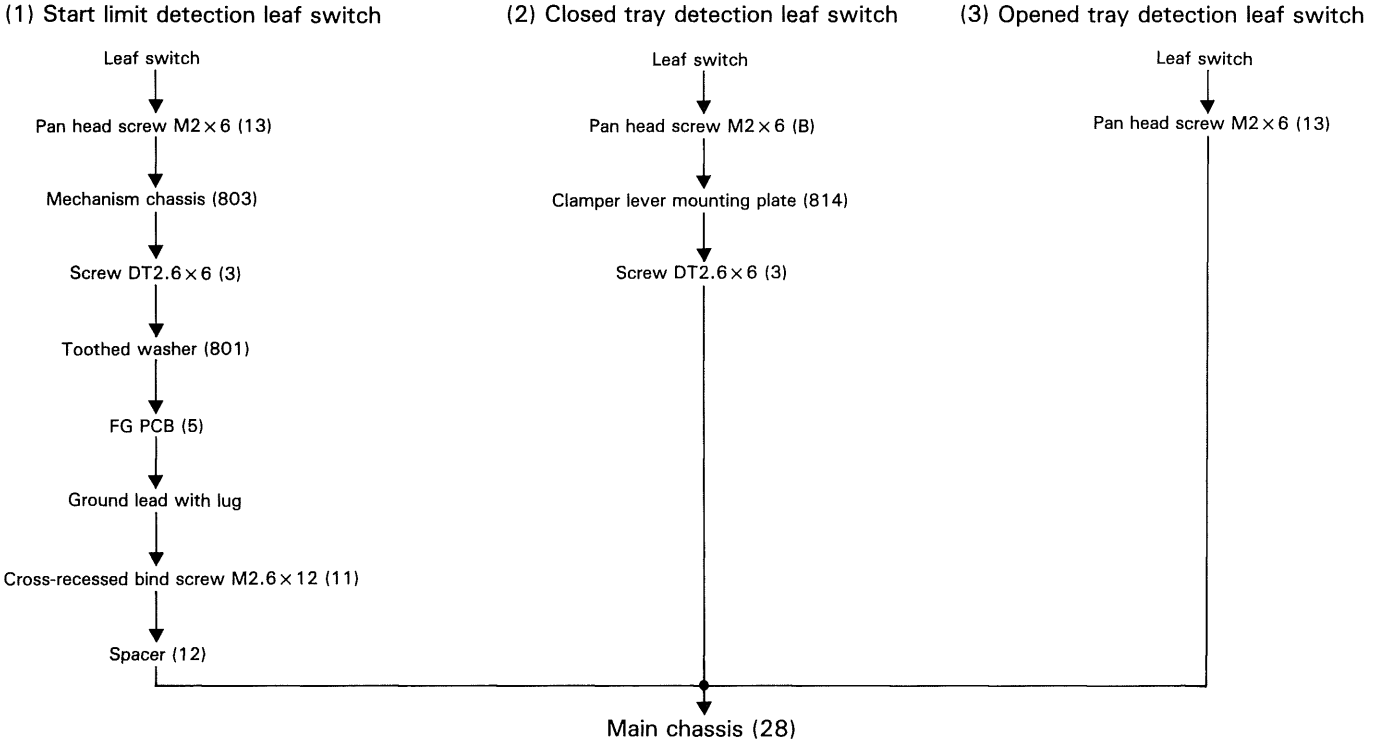
5-2-5 Grounding of each positional detection leaf switch

The respective grounding routes of (1) start limit, (2) closed tray (loading) and (3) opened tray (eject) detection leaf switches are shown in Fig. M19.

(1) Start limit detection leaf switch

(2) Closed tray detection leaf switch

(3) Opened tray detection leaf switch



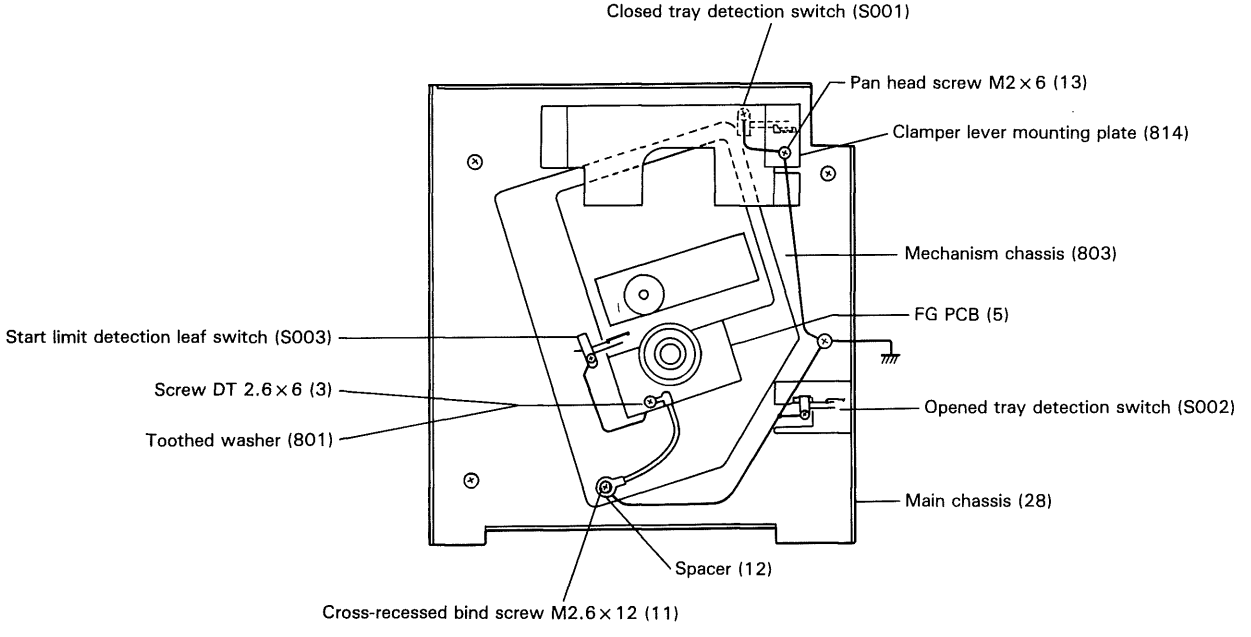


Fig. M19 Ground line of positional detection leaf switches

5. MECHANISM OPERATION

5-3 REPLACEMENT AND REMOVAL OF MAIN COMPONENTS

5-3-1 Replacement of pickup (Figs. M20, M21 and M22)

- Remove screw (61) (M2×8) mounting roller (60) as shown.
- **Be sure to insert a service short pin into laser pickup (38).**
- Disconnect the connectors (5-P socket ass'y (808) and 4-P socket ass'y (807) from laser pickup (38), and desolder the three lead wires.

Note: Make sure to use a grounded soldering iron. Also, ground the chassis in the mechanism section and the body of the service engineer.

- Remove two screws (55) (M3×4) mounting laser pickup (38), and the pickup will be detached.
- Assembly should be carried out carefully in the reverse procedure.

Notes:
- **Short pin should not be taken off from the new pickup till completion of wire connection.**
- **Avoid touching the pickup lens.**
- **When it is difficult to mount the pickup in pickup mount ass'y (816), unfasten the pickup spring (51) at one side for easy mounting. In this case, avoid loosening pickup adjustment screws (82) and (84), because this causes the pickup to go out of adjustment.**
- **When mounting the new pickup, be sure to apply lubricant to the specified points, as shown in Fig. M46. (Refer to 5.4 "Lubricant application points".)**

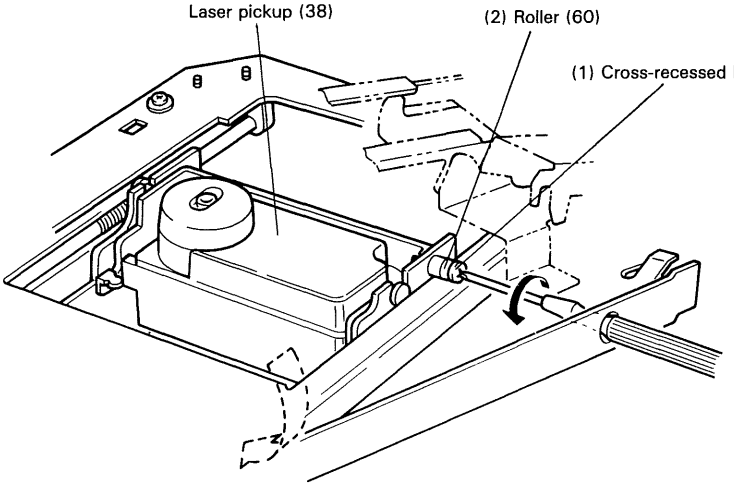


Fig. M20 Replacement of laser pickup (1)

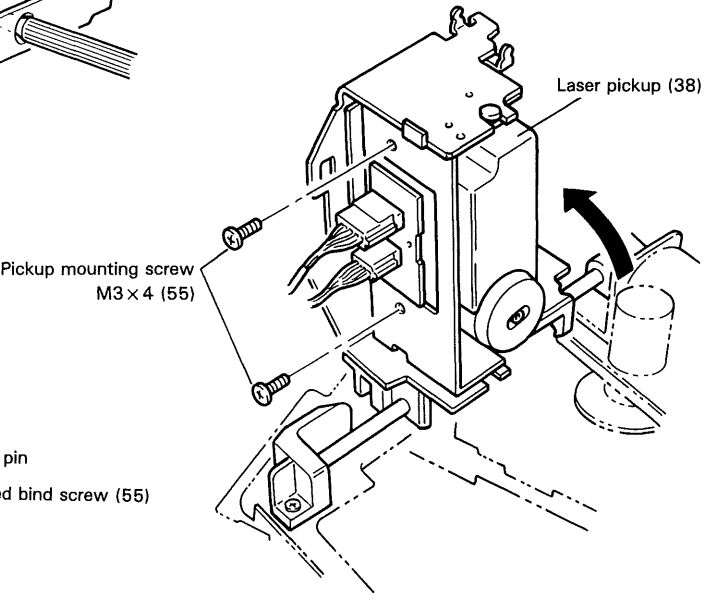


Fig. M21 Replacement of laser pickup (2)

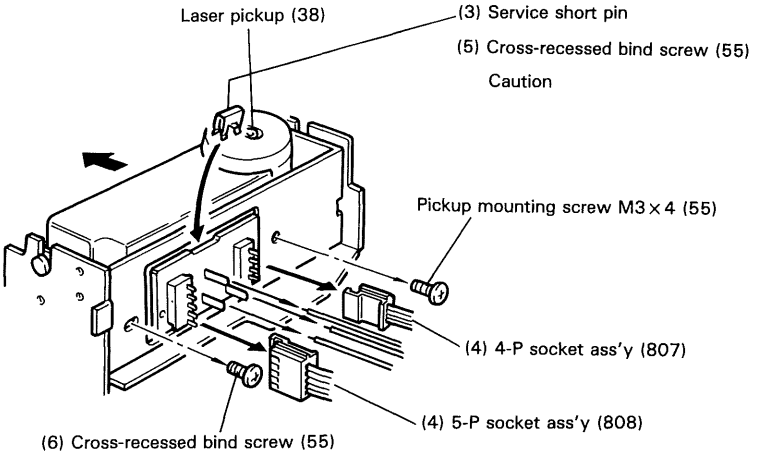


Fig. M22 Replacement of laser pickup (3)

5. MECHANISM OPERATION

5-3-2 Replacement of disc motor on FG PCB

Remove two screws (3) (M2.6×6) mounting the clamper lever mount so that the overall clamper lever mount ass'y can move freely with the lead wires kept connected. (Fig. 1)

↓

Remove push rivet (1) (φ3×3.5) and take out FG cover (800). (See exploded view.)

↓

Remove four screws (3) (M2.6×6) mounting the disc motor.

↓

Desolder the lead wires from FG PCB (5), and the FG PCB will be detached.

↓

Desolder the disc motor lead wires (red and black) from loading motor PCB (27), and disc motor ass'y (10) will be detached. (Fig. M23)

Assembly should be carried out in the reverse procedure.

Note: When securing the disc motor by screws, note that one screw has a toothed washer (4).

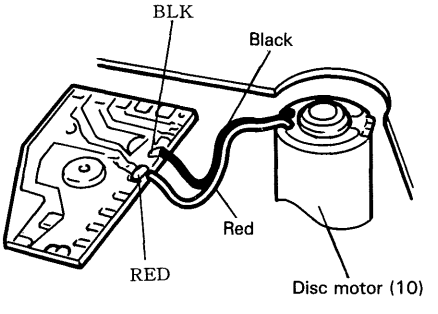


Fig. M23 Replacement of FG PCB and disc motor

5. MECHANISM OPERATION

5-3-3 Replacement of pickup carry motor in pickup slide mechanism section

Remove screw (3) (M2.6×6) mounting the carry motor mount and screw (3) (M2.6×6) mounting the thrust bearing, and separate it into the carry motor section, guide rack section and thrust bearing (17). (Fig. M24)

↓

Remove screw (11) (M2.6×12) mounting the guide rack, and the guide rack section will be separated into the pickup section and guide rack ass'y (19).

Remove screw (22) (M2.6×5) mounting the carry motor, and the carry motor section will be separated into motor mount (23) and motor ass'y (26).

↓

Desolder the terminal section of carry motor ass'y (26).

Assembly should be carried out in the reverse procedure.

Note: Be sure to put gear WH (21) in the drive shaft to its full depth.

Note: In assembly, solder the terminal section with motor polarities set as shown in Fig. M25 (the terminal which has a boss nearby is set to the capacitor side).

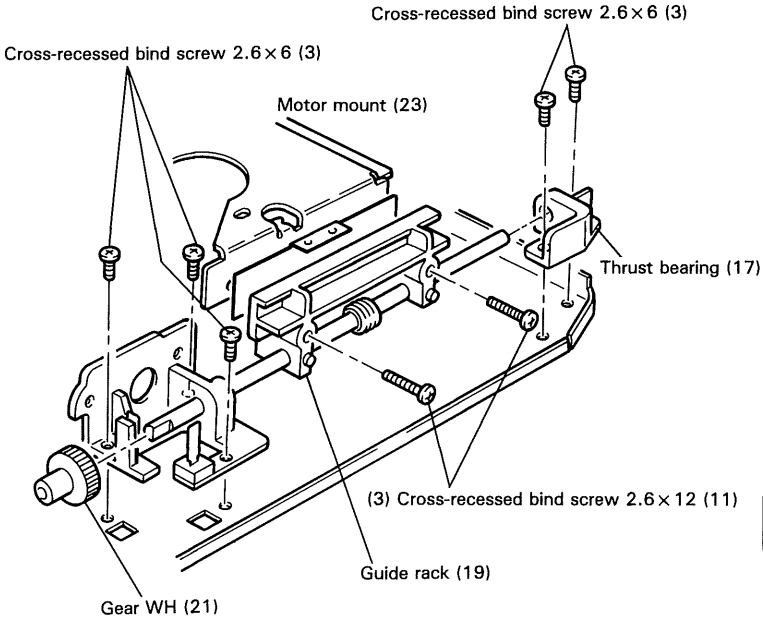


Fig. M24 Replacement of pickup slide mechanism

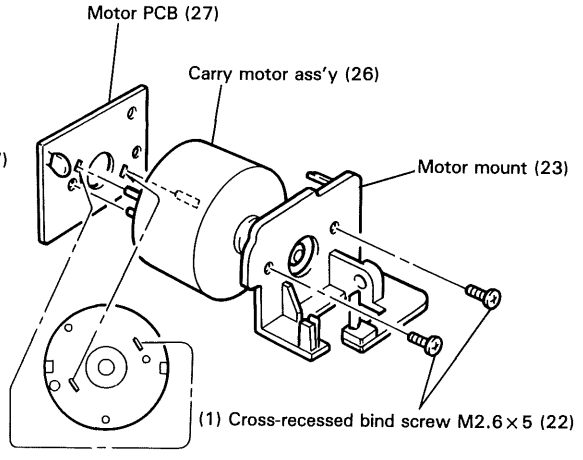


Fig. M25 Replacement of pickup carry motor

5. MECHANISM OPERATION

5-3-4 Replacement of loading motor on loading gear group

Remove screw (3) (M2.6×6) mounting the clamper lever mount so that overall clamper lever mount ass'y (814) can move freely.

↓

Remove screw (11) (M2.6×12) mounting the mechanism chassis so that the overall mechanism chassis ass'y can move freely.

Note: When removing screw (11), be careful not to damage the lead wire (brown) of leaf switch (S001) in overall clamper lever mount ass'y (814).

↓

Remove gear support washer (65) (ϕ2.1), and gear B (66), gear C (67), gear A (70), gear E (68) and gear E ass'y (69) will be detached in that order. When removing gear A (70), slightly raise mechanism chassis ass'y (803).

Note: Take special care in removal of gears, since gear A (70) is extremely susceptible to damage. When removing gear E (68), be careful not to break a gear leg in opening it with tweezers as shown.

↓

Remove screw (71) (M2.6×3.5, black) mounting the loading motor, and loading motor ass'y (74) will be detached.

↓

Desolder the terminal section of loading motor ass'y (74).

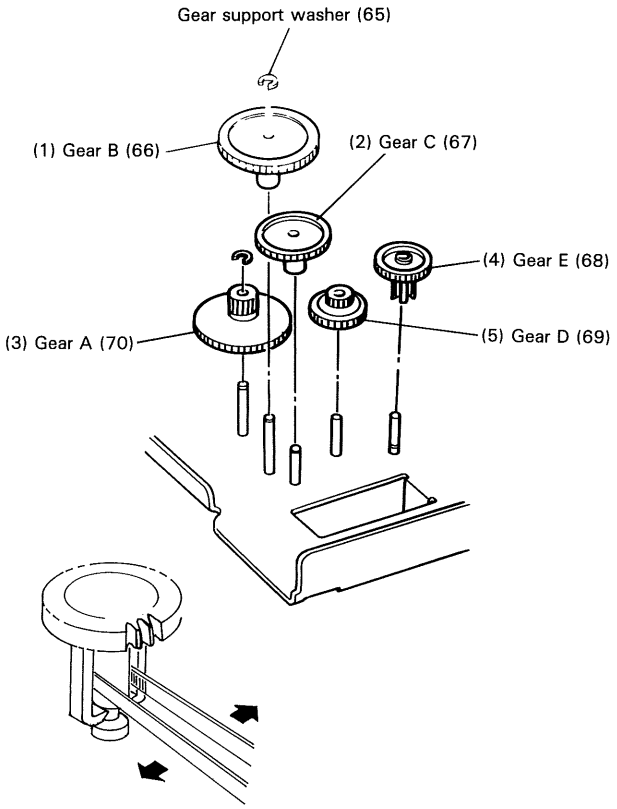


Fig. M26 Replacement of loading gears

Assembly should be carried out in the reverse procedure.

Notes:
- **When putting in gears, be careful not to damage them. Especially, as gear A (70) is susceptible to damage, take adequate care in removal work.**
- **When mounting the loading motor by screw (71), avoid application of excessive turque to the screw, as this may cause a broken thread.**
- **When replacing the loading motor or resoldering it, pay attention to motor polarities. As shown in Fig. M26-B, the hole section in the panel side is the specified soldering point and motor mounting location.**

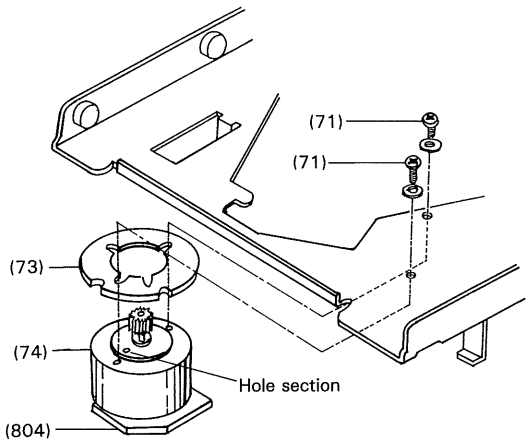


Fig. M26-B

5. MECHANISM OPERATION

5-3-5 Replacement of tray

Remove the four tapping screws of the panel reinforcement plate and the four red tapping screws securing the mechanism to the unit as shown in Fig. M28, restore the tray to the state that it is nearly housed in, then lift up the mechanism in its rear side as shown in Fig. M28-a. The metal fixture (right) of the rail will then be detached sideways.
Detach this metal fixture, then restore the mechanism to the original location, and the tray can be pulled out forwards manually.

Note: The tray can be detached with a short shaft screwdriver for M2.6 without removing the above eight screws as shown in Fig. M27.

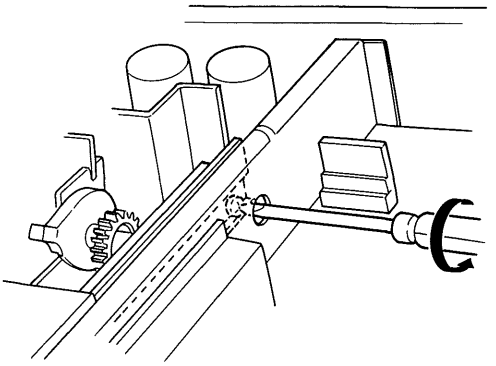


Fig. M27 Removal of tray

Draw out the tray in its opening direction, slowly.
Assembly should be carried out in the reverse procedure.

Notes:
- **When putting in the tray, make sure that gear C is engaged with the drive rack.**
- **Be careful not to damage the rollers of main chassis ass'y (28) by the edges of the rails.**

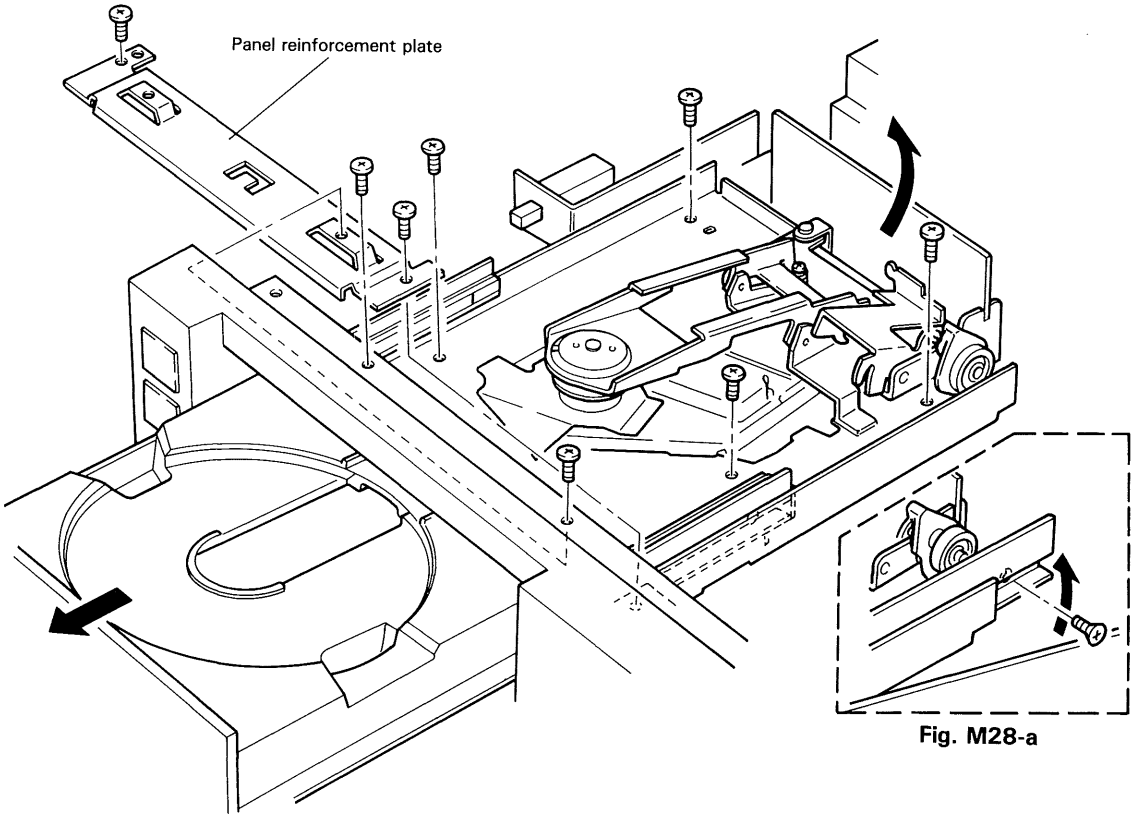


Fig. M28-a

Fig. M28 Removal and replacement of tray

5. MECHANISM OPERATION

5-3-6 Replacement of mechanism chassis rubber cushion

Remove screw (3) (M2.6×6) mounting the clamper lever mount so that overall clamper lever mount ass'y (814) can move freely. (Fig. M3)

↓

Remove screw (11) (M2.6×12) mounting the mechanism chassis so that mechanism chassis ass'y (803) can move freely.

Note: Be careful not to damage the lead wire (brown) of leaf switch S001 in the clamper lever mount.

↓

Detach spacer (12).

↓

Detach cushion (14) by gently pushing it from above with mechanism chassis ass'y (16) slightly raised.

Note: When raising mechanism chassis ass'y (16), take adequate care not to damage gear A (70) by carry motor PCB (87).

Assembly should be carried out in the reverse procedure.

5-3-7 Removal of head amplifier PCB

Remove screw (3) (M2.6×6) of head amplifier PCB mounting metal fixture (30) so that head amplifier PCB ass'y (812) can be detached from the mechanism section.

↓

Be sure to insert the service short pin to laser pickup (38). (Fig. M22)

Note: Make sure to use a grounded soldering iron. Also, ground the chassis in the mechanism section and the body of the service engineer.

↓

Desolder the wires and pull out the connectors from head amplifier PCB ass'y (812).

Assembly should be carried out in the reverse procedure.

Note: Short pin should not be taken off from the pickup till completion of connection.

5-3-8 Replacement of clamper lever mount

Remove screw (3) (M2.6×6) of head amplifier PCB mounting metal fixture (30) and screw (3) (M2.6×6) of clamper lever mount (814). (Fig. M3)

↓

Remove pan head screw (13) (M2×6) of leaf switch S001 taking care not to damage the brown wire, and the clamper lever mount will be detached. (Fig. M10)

↓

Remove E-ring (54) (ϕ3), and clamper gear (53) will be detached.

Assembly should be carried out in the reverse procedure.

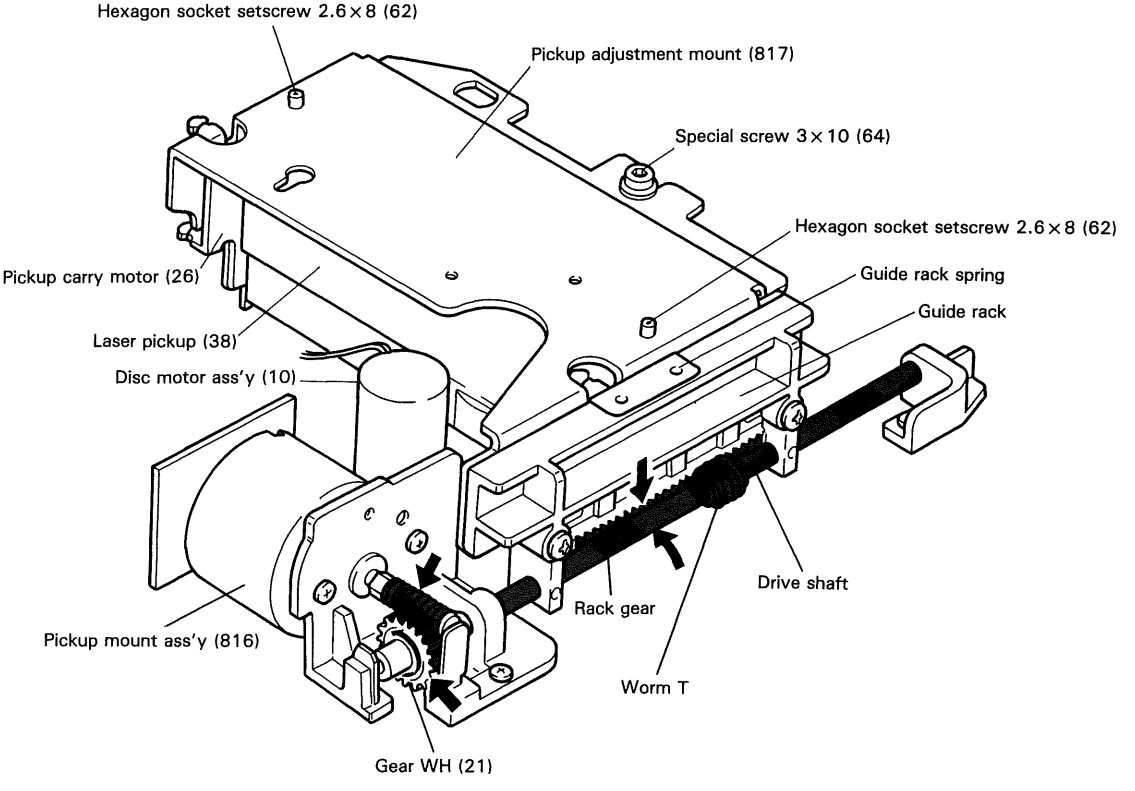
5. MECHANISM OPERATION

5-4 LUBRICANT APPLICATION POINTS

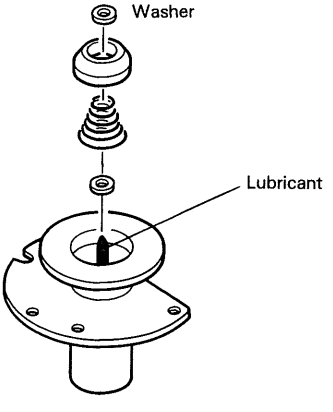
When replacing a component, when the operation of each section goes out of order, check that lubricant (300,000 unit silicon oil) has been applied to the following points:

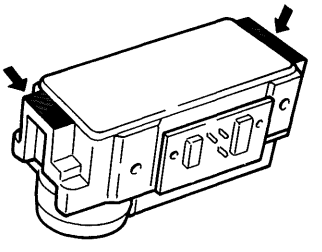
(1) Worm and gear WH in carry motor (Fig. M47)
(2) Drive shaft (300,000 unit silicon oil) (Fig. M47)
(3) Worm T and guide rack (300,000 unit silicon oil) (Fig. M47)
(4) When replacing the pickup, be sure to apply 300,000 unit silicon oil between the pickup and its support screw. Without such application, note that the pickup cannot be adjusted.
(5) Sliding section between pickup roller and mechanism chassis (300,000 unit silicon oil)
(6) Cam section of clamper gear (300,000 unit silicon oil)
(7) Disc motor shaft and center ring (300,000 unit silicon oil) (Fig. M49)
(8) Cam section and rack spring sliding section in tray (300,000 unit silicon oil)
(9) Lock lever and lock pin of tray
(10) Sliding section between clamper lever and lock lever adjustment screw

Note: 300,000 unit silicon oil (Parts No. W01-9991-00)



Lubricant application point





5. MECHANISM OPERATION

5-5 CLAMPER LEVER HEIGHT ADJUSTMENT

When the disc motor does not rotate even if a disc is loaded, or when no data TOC is read even if the disc motor rotates (e.g. it rotates infinitely), or when a friction sound occurs in rotation of the disc motor, the clamper lever may be in contact with the clamper.

a) In this case, adjust by turning the height adjustment screw (Fig. M39-a) so that the ratio of clearances A and B is A:B = 2:3 with the disc clamped as shown in Fig. M39-b.

b) When this problem is not desolved even by the method mentioned above, turn the clamper and see if the clearance (C), which can be checked through the notched section of the clamper, is almost the same at several points when turning.
When the clearance is smaller at right and left, correct it by pushing the clamper lever manually. (Fig. M40)

c) Lock lever ass'y (813) is also provided with an adjustment screw which is used as in clamper lever height adjustment (Fig. M39-d) with tray open.
This screw is used in adjustment only when the clamper creates friction with tray A in loading of disc or when sound occurs by the clamper striking the top case.
As shown in Fig. M41, adjust this screw so that the clamper is kept from striking the top case also meeting the application of tray A to clamper clearance (d) ≥ 1 [mm].

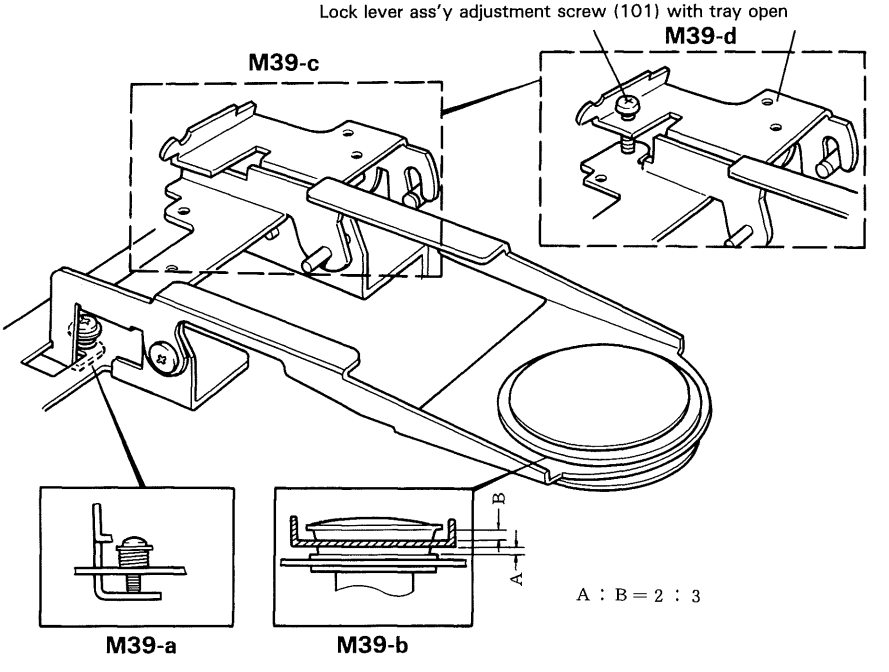


Fig. M39 Clamper lever height adjsutment

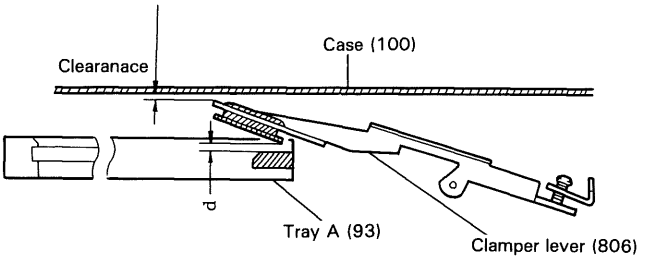


Fig. M41 Clamper lever height adjustment with tray open

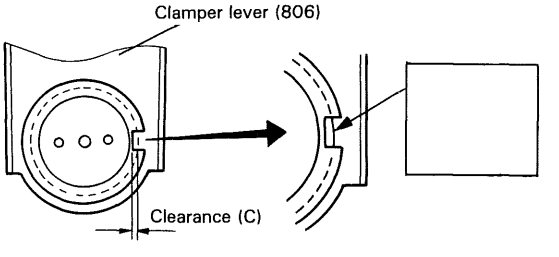


Fig. M40 Clamper lever-plate clearance check

5. MECHANISM OPERATION

5-6 WIRE CONNECTION AND BUNDLING

1. Wire connection for motors and leaf switches is as shown in Fig. M42.
   1) Connect the black, yellow, red and orange wires from the 4-P socket to BLK, YEL, RED and ORG wires, respectively.
   2) Connect the blue wire of the 3-P socket to the blue wire of the start limit detection leaf switch through the loading motor PCB, the brown wire to the brown wire of the closed tray detection leaf switch through the same PCB, and the gray wire to the gray wire of the opened tray detection leaf switch directly.
   3) Connect the red and black wires of the disc motor to the D.RED and D.BLK wires in the loading motor PCB, respectively.

   Note: When wire connection is made as instructed in paragraph 1) and 2), the red wire of the disc motor is connected with the black wire of the 4-P socket, and the black wire with the red wire.
2. Wiring is performed as shown in Figs. M43 - M46.
   1) Perform wiring of the motor PCB exactly as shown in Fig. M43. In this case, note the following three points:
      a) Slacken the wire indicated by arrow [A].
      b) Slightly bend the section indicated by arrow [B] in the direction in which the wire is put in.
      c) Bring the locking part of the wire band upward indicated by arrow [C], as shown.
   2) Perform wire bundling in the rear of the main chassis exactly as shown in Fig. M44. In this case, the number of wires to be bundled in the locking part is 8, and that in the head amplifier PCB is 9.
   3) In wiring the pickup section, solder the red, black and yellow wires exactly as shown in Fig. 45, and secure these three wires by a wire clamp.
   4) In wiring the head amplifier PCB ass'y, solder the red, black and yellow wires exactly as shown in Fig. M46. In addition, make sure that no contact occurs between any two of the transistors, coils and capacitors shown in Fig. M46.

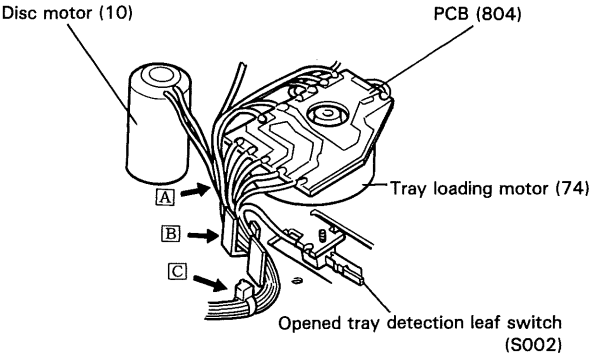


Fig. M43 Wiring of motor PCB

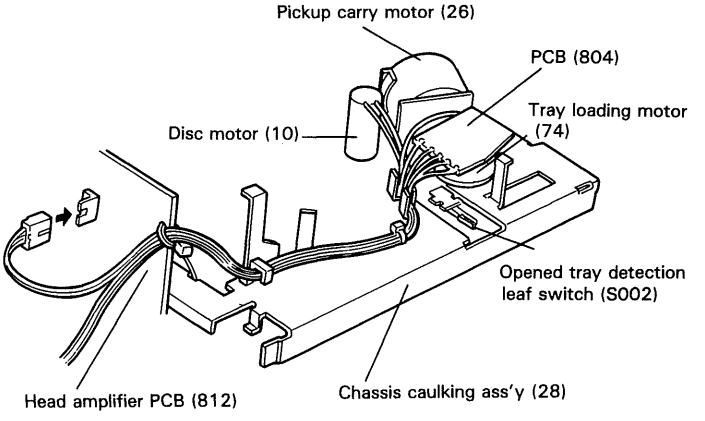


Fig. M44 Wire bundling in rear of main chassis

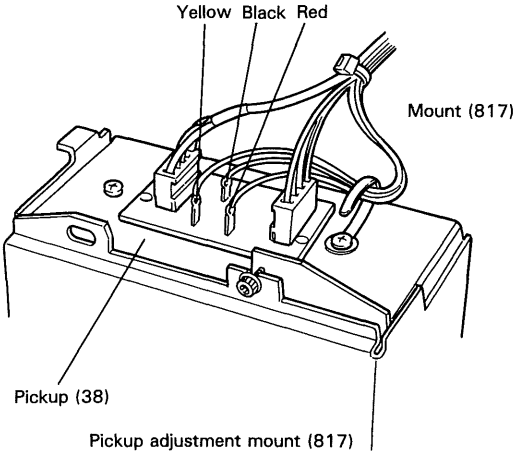


Fig. 45 Wiring of pickup section

5. MECHANISM OPERATION

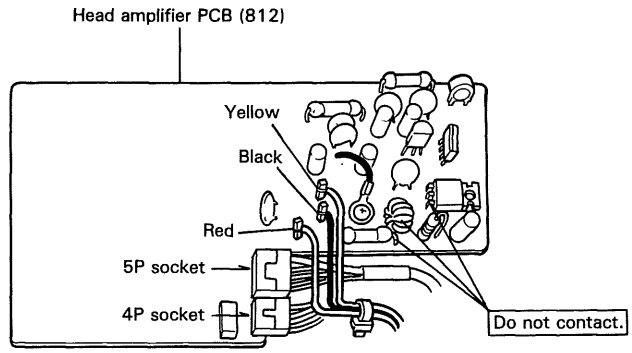


Fig. M46 Wiring of head amplifier PCB ass'y

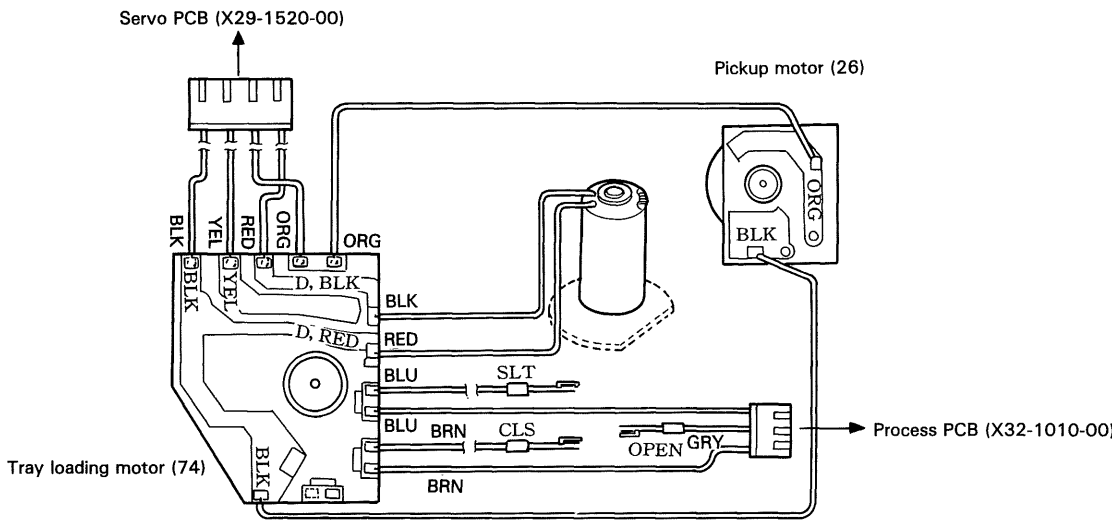


Fig. M42 Connections for motors and leaf switches

14. SPECIFICATIONS

DP-1100B

Compact disc player

Disc loading system .....Linear skate disc loading mechanism
Frequency response .....2 Hz to 20 kHz, ±0.5 dB
Dynamic range .....95 dB or more
Signal-to-noise ratio .....95 dB or more
Total harmonic distortion .....Less than 0.0015% (1 kHz)
Channel separation .....90 dB or more (1 kHz)
Wow and flutter .....Below measurable limit
Output level .....2 V
Output impedance 600Ω
Sampling frequency .....44.1 kHz
Quantization .....16 bit linear quantizing/channel
Spindle speed .....200 to 500 rpm
Pickup .....Semiconductor laser (GaAlAs)
Error correction .....C.I.R.C
Tune selection .....TNO (Music No.), INDEX (Index No.)
Number of tune search .....Up to 99
Access time .....Average 2 seconds
Number of memory 16
Repeat play .....Endless
Power supply .....AC 120 V, 60 Hz (USA and Canada)
AC 120 V to AC 220/240 V, 50/60 Hz (Others)
Power consumption .....20 W (USA),
23 W (Others)
Dimensions .....440(W) × 88(H) × 310(D) mm
Weight .....6.8 kg

Remote control unit

System .....Infrared control
Wave length; 930 nm
Effective distance .....4 m
Effective angle .....±30° from the center axis
Dimensions .....140(H) × 54(W) × 12(D) mm
Batteries .....AAA or R03 × 2 (option)
Weight .....50 g (without batteries)

DP-1100II

Compact disc player

Disc loading system .....Linear skate disc loading mechanism
Frequency response .....2 Hz to 20 kHz, ±0.5 dB
Dynamic range .....95 dB
Total harmonic distortion .....0.0015% (1 kHz)
Channel separation .....90 dB (1 kHz)
Wow and flutter .....Below measurable limit
Output level .....2 V
Sampling frequency .....44.1 kHz
Quantization .....16 bit linear 1 channel
Pickup .....Semiconductor laser
Power supply .....AC 120 V, 60 Hz (USA and Canada)
AC 120 V to AC 220/240 V, 50/60 Hz (Others)
Power consumption .....23 W
Dimensions .....W 440 mm (17-5/16″)
H 88 mm (3-15/32″)
D 310 mm (12-7/32″)
Weight .....6.8 kg (15 lb)

Remote control unit

System .....Infrared control
Wave length; 930 nm
Effective distance .....6 m
Effective angle .....±30° from the center axis
Dimensions .....140(H) × 54(W) × 12(D) mm
Batteries .....AAA or R03 × 2
Weight .....50 g (without batteries)

Kenwood follows a policy of continuous advancements in development. For this reason specifications may be changed without notice.

Kenwood poursuit une politique de progrès constants en ce qui doncerne le développement. Pour cette raison, les spécifications sont sujettes à modifications sans préavis.

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